Recent Problems of VLSI Physical Design Automation

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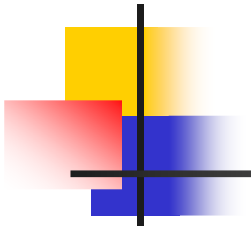
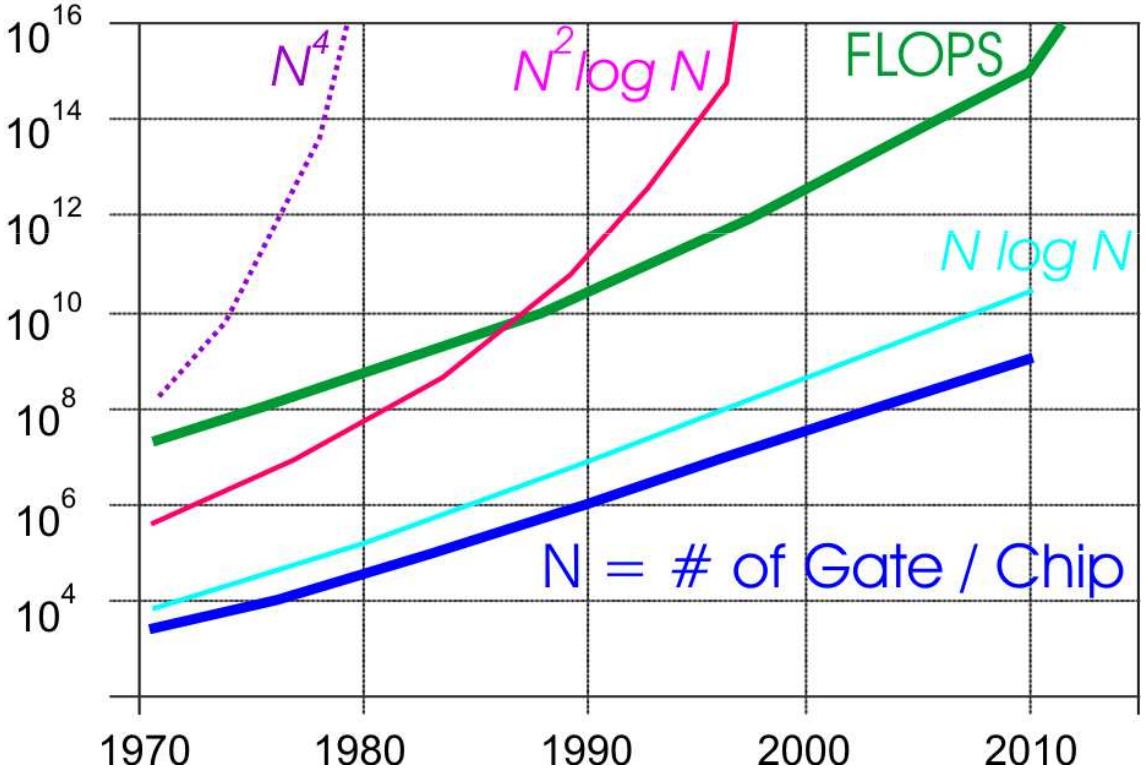


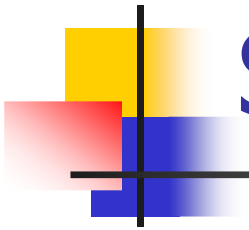
Outline

- Time-to-Market
- Chip Area
- Timing-Aware Design Flow
- Power Consumption
- Deep Submicron Effects
- OPC (Optical Proximity Correction)
- DFM (Design-for-Manufacturability)
- Optimization Techniques

Time-to-Market

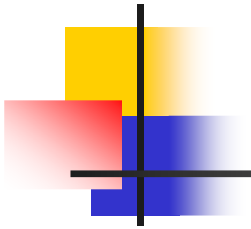
- IC design cycle time frame is ~ 1 Year





Solution

- Reducing complexity of algorithm
  - $O(n!) \rightarrow O(n^4) \rightarrow O(n^2 \log n) \rightarrow O(n \log n)$
  - O(n log n) can be achieved by heuristic methods
- Hierarchical partition
  - Trade-off "Performance vs. Quality"
- R&D of principal new design methodology
  - Going out of Standard Cell methodology



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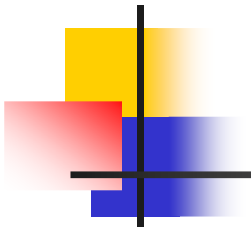
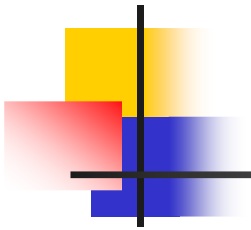


Chip Area

- Market: Chip cost must be reduced
- Functionality should be intelligent
  - Need to use embedded real-time SW
- Operation frequency have to be higher
- MOS channel length have to be shorter
- FAB needs to decrease min dimension
  - 1 kGate cost: 65 nm < 45 nm
- Chip cost is increasing!

Conclusion: Chip area must be minimized



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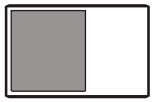
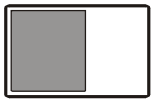
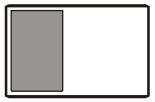
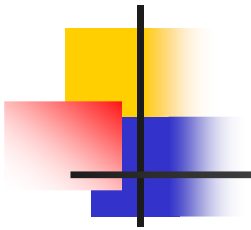
Timing-Aware Rate

Flow Stage	Today	Tomorrow	Future
Partition	X	?	
Floorplanning			
Placement			
Global Routing			
Detail Routing			
Post Process			

Timing Estimation Models

- Detail Routing: wire geometry
  - $t_{delay} = f(L_{wire}, N_{VIA}, N_{JOG})$
- Global Routing: SMT topology
  - $t_{delay} = f(L_{wire}, N_{JOG})$
  - Cost_SMT $\rightarrow$ (Cost_SMT, Radius_SMT)
- Placement: SMT cost estimation
  - Cost_SMT $\rightarrow$ (Cost_SMT, Radius_SMT)
- Partition: No real solution, subject of R&D



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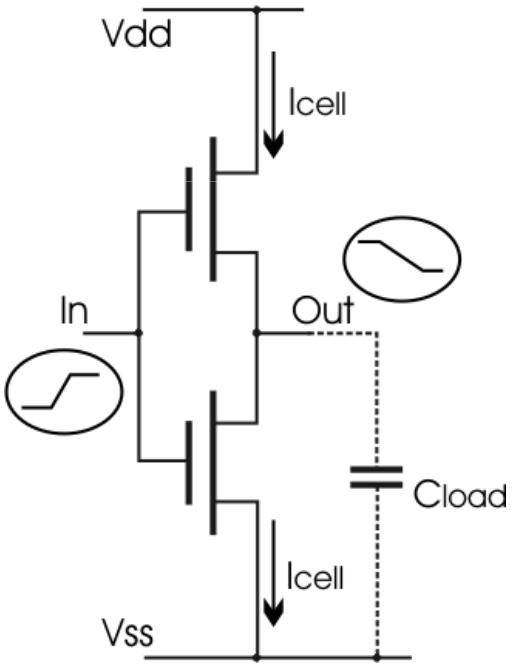
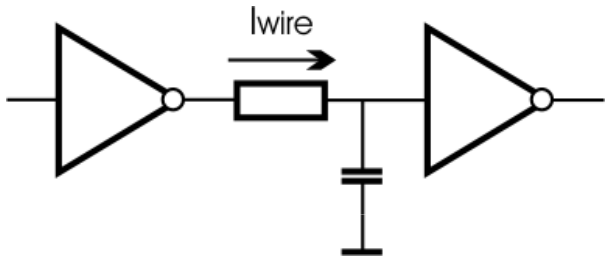
Power Consumption

- $P_{chip} = P_{leakage} + (P_{cell} + P_{wire})$





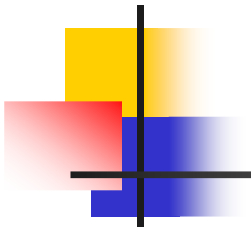
$P_{leakage}$ is depend on StdCell layout

$P_{cell} = f (C_{load}) = f (L_{wire})$

$P_{wire} = f (R_{wire}) = f (L_{wire})$

$P_{dynamic} = P_{cell} + P_{wire} = f (2 \times L_{wire})$

$L_{wire} \rightarrow$ min



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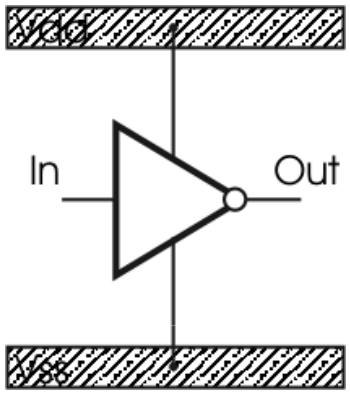
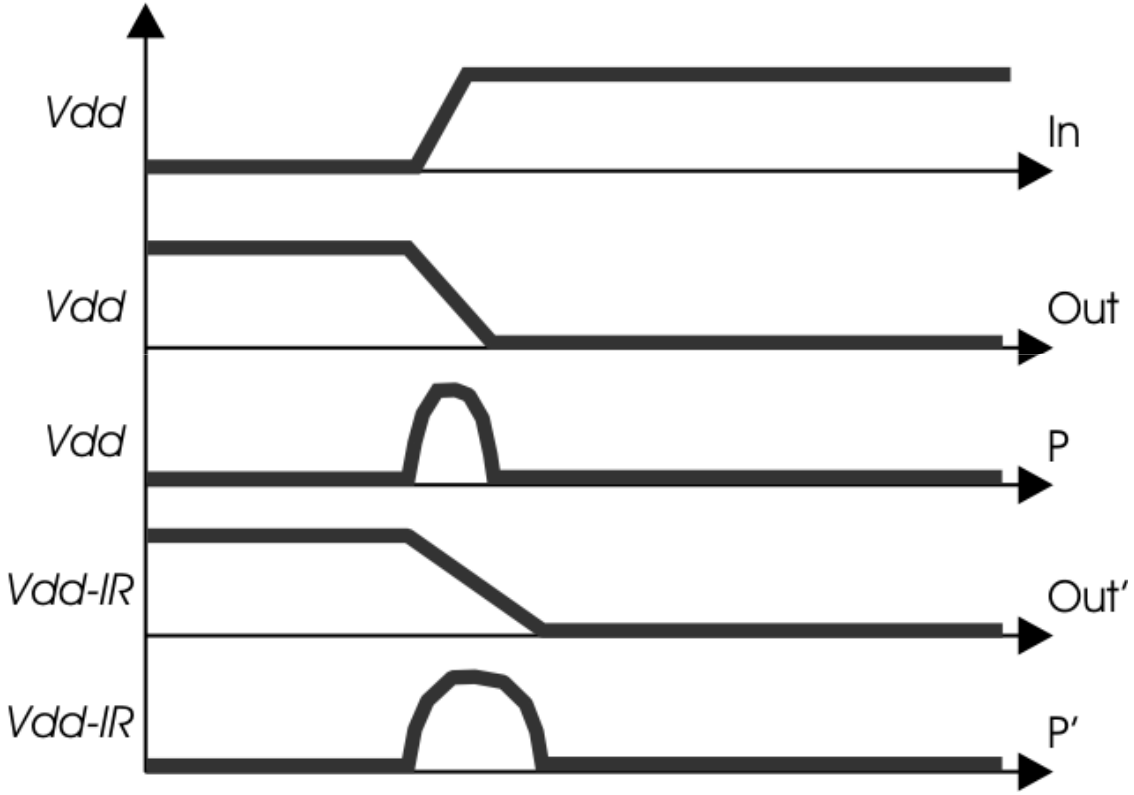
Deep Submicron Effects

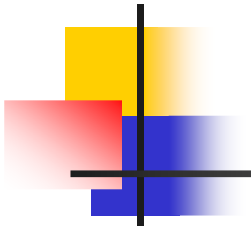
- Cross-Talk
- IR-drop
- Electromigration

- Today: Routing then Find&Repair
- Tomorrow: Find&Repair during detail routing

Cumulative IR-drop







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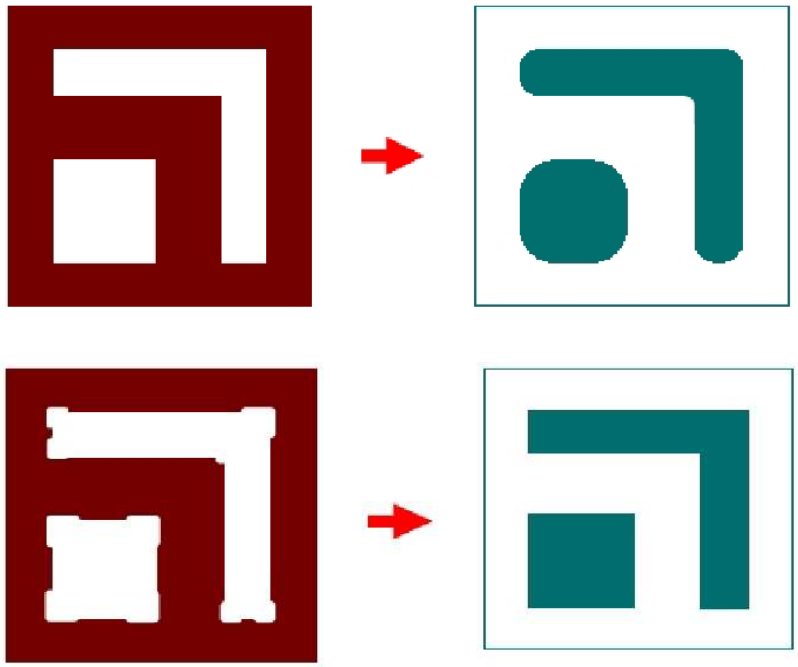
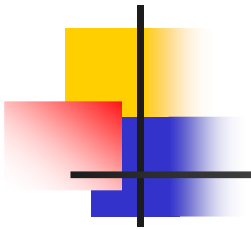
Optical Proximity Correction



- Rule-based OPC: post processing, new design rules
- Model-Based OPC



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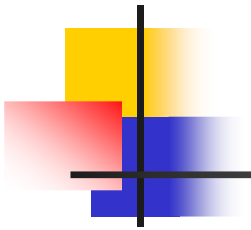
Design-for-Manufacturability

Year	Layout Designer's point
1980	DFM?! What's this?
1990	Agree, I need to fix "antenna".
2000	It seems DFM impacts to yield. For first silicon it doesn't matter. Further I'll optimize design to DFM.
2007	DFM recommendation was ignored, FAB reports 30% yield. Why it's so low?
2010	You didn't satisfy DFM! Yield = 0.001%



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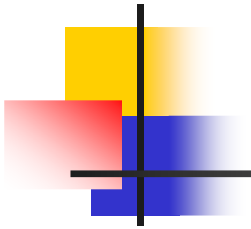
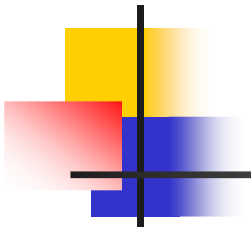


Optimization Techniques

- Deterministic Methods
  - Greedy algorithms (Bisection)
  - Iterative algorithms (Kernigan-Lin)
- Heuristic Techniques
- Global Optimization Techniques
  - Simulating Annealing
  - Simulating Evolution
- Mathematical Methods
  - Integer-Linear Programming
  - Non-Linear Programming



Conclusion

- Actual criteria: area, timing, power, DFM, signal integrity, density
- Actual metrics: area, wire length, number of vias, number of jogs, congestion
- Moving to native multi-objective optimization
- Moving to R&D new design methodology