Reliability Implications of Bias Temperature Instability in Digital ICs

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Reliability Implications of Bias Temperature Instability in Digital ICs,
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Sang Phill Park, Kaushik Roy, Kunhyuk Kang

Agenda

- Introduction
- NBTI mechanism
- NBTI in random logic circuits
- NBTI in 6T SRAM cell
- Reliability-aware circuit design
- Conclusion

Introduction

- SUCCESSFUL DESIGN of Digital ICs
  - Silicon area, speed, testability, design effort, and power dissipation.
- Is the physical and electrical properties of a transistor deterministic and hence predictable over its life time ?
- Negative Bias Temperature Instability (NBTI)
  - Negative bias, high temperature, time.
  - PMOS specific transistor aging effect.
  - PMOS biased in inversion.
  - Holes near Si/SiO_2 interface.

Is NBTI a major reliability concern ?

- Major reliability challenge in nanoscale CMOS technology.
  - Scaling - ultrathin oxide devices and increased electric field.
  - Increased chip operating temperature.
- Results in threshold voltage increase.
- Degrades mobility, drain current, transconductance.
- Introduce extra delay in circuit over its life time.
  - Circuit/system may fail to meet its timing specifications.
  - Max frequency of operation reduces.
  - Reduced life time.
  - Introduce safety concerns in a critical embedded system.

Some NBTI facts ..

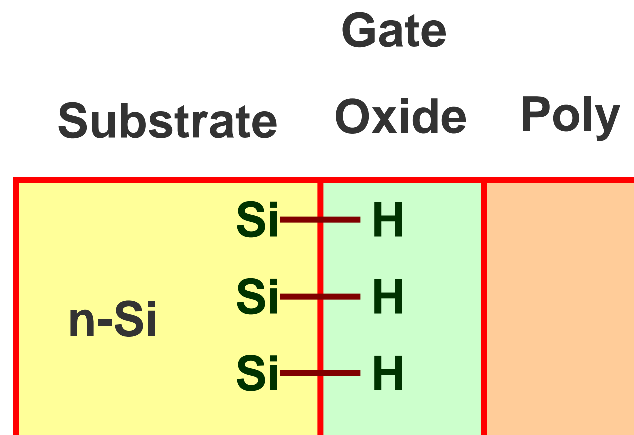
- Not yet fully understood !
- 25-30 % increase in V_{TH} over 10 years.
- Wide variation depending on specific topology and operating condition.
- Delay between the release of stress and measurement is very important.

NBTI Mechanism

- Reaction diffusion (RD) model.
- Combined effect of electric field, temperature and holes.
- Interaction of inversion layer holes with hydrogen-passivated Si atoms.

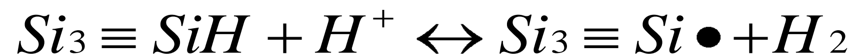
$$Si_3 \equiv SiH$$

- Breaking of Si-H bonds at the SiO_2/Si substrate.

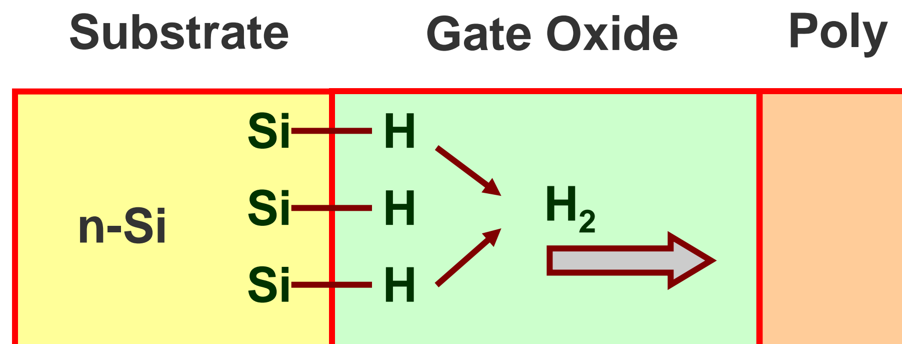


Reaction Diffusion model

- Holes from the inversion layer under sufficient temperature can break Si-H bonds.
  - Results in dangling bonds or interface traps.
- The H_2 diffuses away from the interface into the oxide or poly-Si gate.
- H_2 diffuse back to the interface when the stress voltage is removed.



$$Si_3 \equiv SiH + H^+ \leftrightarrow Si_3 \equiv Si\bullet + H_2$$



RD based V_{TH} model

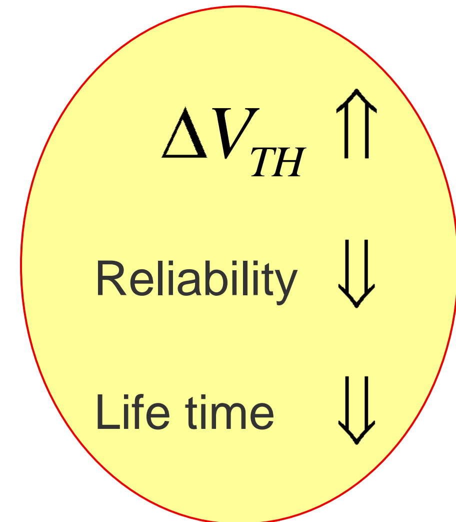
- ❑ Interface traps increase the device V_{TH}.

$$\Delta V_{TH} \approx \frac{q \bullet N_{it}(t)}{C_{ox}} \approx f_{AC}(S_p) \bullet K_{DC} \bullet t^{n}$$

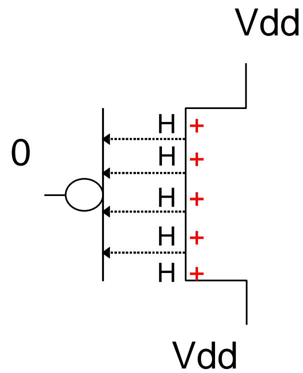
- ❑ N_{it} is the density of interfacial traps
- ❑ K_{DC} is a technology, VDD, device geometry, oxide nitrogen concentration and temperature dependent constant.
- ❑ Sp is signal probability, represents the fraction of time when input is high.

Impact of DC and AC stress on V_{TH}

- DC stress
  - Power law, $\Delta V_{TH} \sim t^n$
  - On-the fly measurements : n ~ 1/6.
  - Measurements with delay : n ~ 1/4.
- AC stress
  - Stress phase and Recovery phase.
  - n ~ 1/6
  - Degradation scaled by a signal probability dependent function.

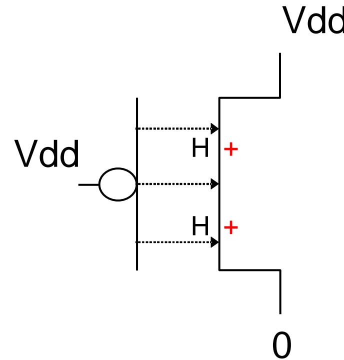


NBTI degradation under AC and DC stress



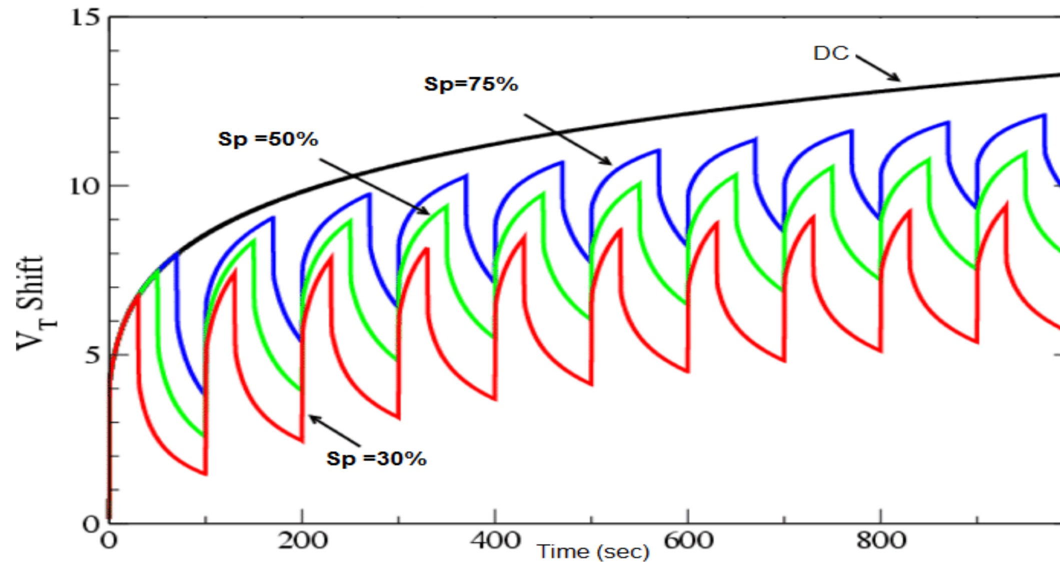
Stress: $V_{gs} = -V_{dd}$

Increase in N_{it} and V_{TH}



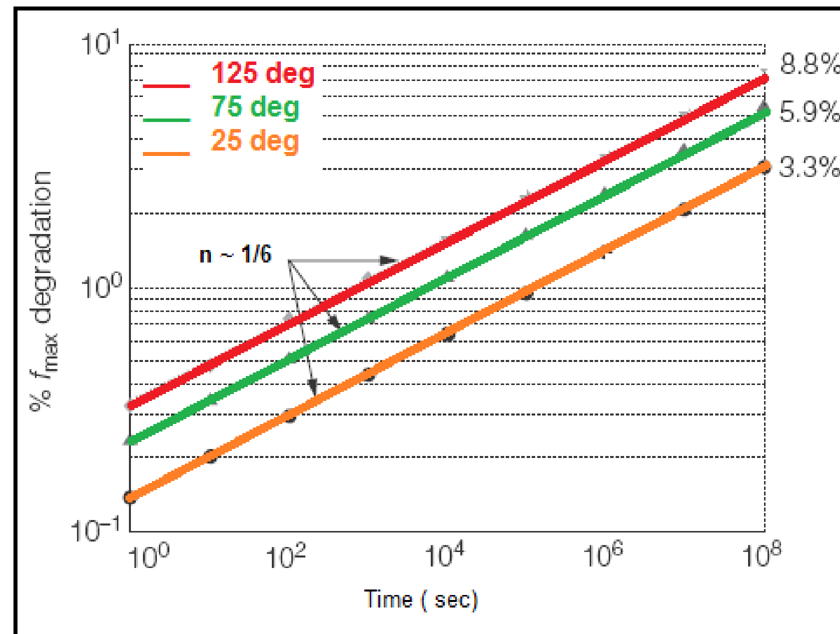
Recovery: $V_{gs} = 0$

Decrease in N_{it} and V_{TH}

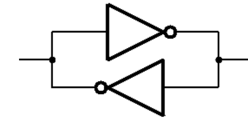


NBTI in random logic circuits

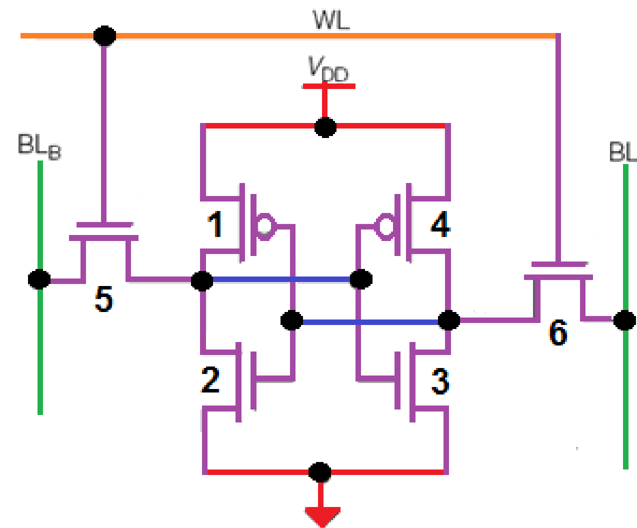
- Delay degradation.
- Increased V_{TH} reduces drive current and thus increases individual gate delays.
- In a timing path with rising and falling transitions, the impact of NBTI is less.



6T SRAM cell



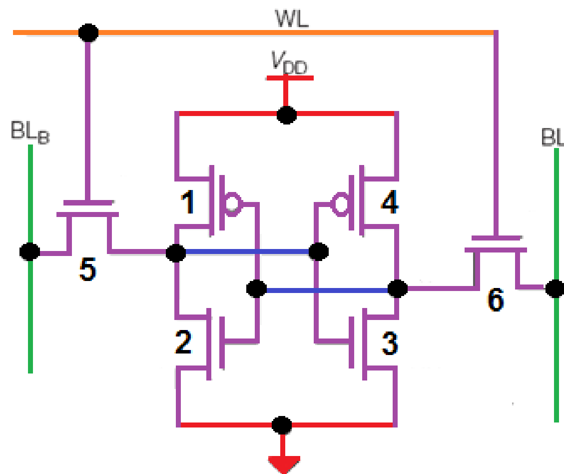
- Bit stored in cross coupled inverters.
- Two stable states - 0 and 1.
- In standby, cross coupled inverters reinforce each other.
- Two access transistors.
- Read and write can be done by proper assertion of BL and WL.
  - BL – Bit Line
  - BL_B – not (Bit Line)
  - WL – Word Line

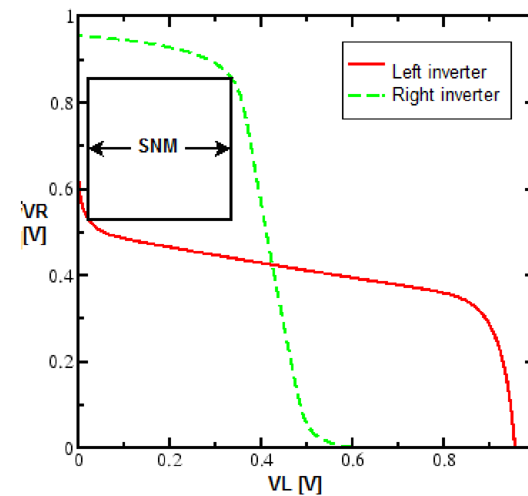


Source: http://www.iue.tuwien.ac.at/phd/entner/node34.html

NBTI in 6T SRAM cell

- Degradation to PMOS.
- Local mismatch among Transistors can lead to failures.
- NBTI degradation can severely damage SRAM read stability.
- Static Noise Margin (SNM) of an SRAM cell decreases.
- Read failure probability increases.



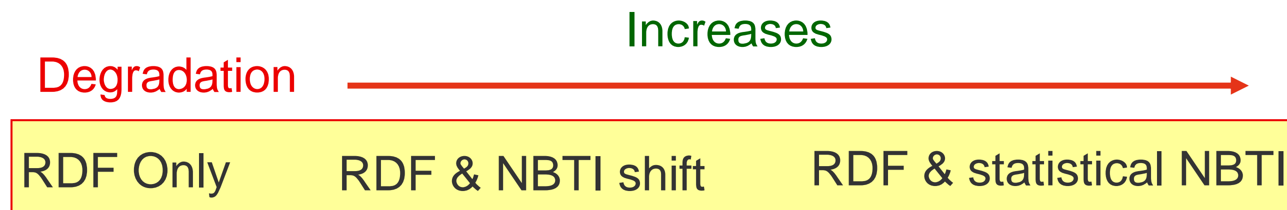


Statistical variation in NBTI

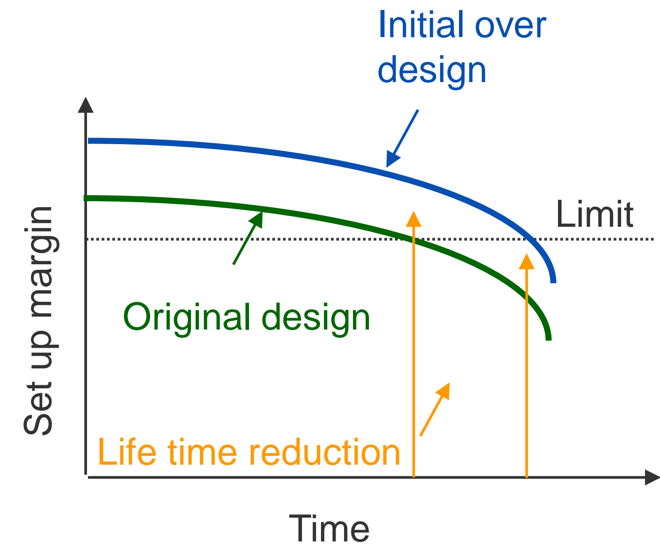
- Transistor mismatch originates from random dopant fluctuation (RDF) as V_{TH} variation.
- NBTI combined with random process variation has greater effect.
- With aggressive scaling of device dimensions, breaking and repassivation of Si-H bonds in the channel experience stochastic fluctuations.

$$\sigma_{VTH} = \sqrt{\sigma_{RDF}^2 + \sigma_{NBTI}^2(t)}$$

  - σV_{TH} is the total V_{TH} variation after time t.



Reliability aware Circuit Design



- ❑ Delay guard banding.
- ❑ Sizing technique
  - WC sizing method. (Worst case)
  - Optimal sizing – Less area over head.
- ❑ Synthesis
  - Worst case NBTI synthesis.
  - Signal probability based synthesis (SP).
- ❑ Stand-by VDD scaling – depends on standby time of memory.
- ❑ On chip sensors – Area and power over head.

Conclusion

- Successful IC design is a complicated optimization problem and transistor reliability could be an even more severe problem in future technology nodes.
- With Hf based promising high-k dielectrics, PBTI also comes out as a major reliability challenge apart from NBTI and other reliability concerns like Hot Carrier Injection.
- Reliability-aware design of digital circuits and memories is essential for future nanotechnologies to ensure robust and stable products.