Research of Integrated Digital Decimation Filters

D. Zhukov, MIET

[1] In digital signal processing, **decimation** is a technique for reducing the number of samples in a discrete-time signal. Decimation is a two-step process:

1. Low-pass anti-aliasing filter
2. Downsampling

An example of decimation: the frequency of a recorded sound can be raised an octave by eliminating every other sample without changing the sampling rate. This will result in aliasing if the sound contains overtones whose (doubled) frequency will exceed half the sampling rate. Decimation aliasing can be avoided by eliminating those overtones.

The same principle applies to eliminating samples at other intervals.

[2]A decimation filter can be realized by cascading several stages. The decimation ratio must be factored into the product of integer numbers. Of course before of each cascade should be placed low pass filter for aliasing exception. And on this slide show structure of multistage decimation filter.

[3] Main types of decimation filters is CIC-filters and Halfband-filters. PROs and CONs both types show on next slide. Main advantage of Halfband-filters is flatter frequency response than CIC-filters. But they contain in its structure multiplies whereas CIC-filters contains only adders and subtracters. The general filter used in PDC designs is a halfband product. The halfband is also typically implemented as a fixed coefficient filter, however it also represents a less efficient implementation than the CIC.

[4] On the next slide I show frequency response both types filters. It is visible that frequency response of halfband-filters more smooths that at the CIC-filter while CIC-filters have multiple zero-areas with multiple frequency bands.

[5] In present I investigated work of CIC-filters as simplest in design, therefore further I will tell about them. Basic characteristics of CIC-filters: **N** - number of CIC stages, **R** – decimation rate change, **M** - differential delay in the comb section stages of the filter. The implementation of this filter response with a clever combination of comb filter sections, integrator sections, and downsampling for decimation give rise to the hardware-efficient implementation of CIC-filters. Also on this slide shown basic architecture of filter.

[6] On the next thirds slides shown dependences of the frequency response from main parameters. This shows the effect of the differential delay **M** on the magnitude response of a filter with 3 stages (**N** = 3) and a sample rate change **R** = 7. Besides the effect on the placement of the response nulls, increasing **M** also increases the amount
of attenuation in side lobes of the magnitude response.

[7] The effect of **R** on the magnitude response can be seen in this figure. In essence, increasing the rate change increases the length of the cascaded unit-amplitude, rectangular window of length **R*****M**. This results in an increase in attenuation and decrease of the width of the response side lobes.

[8] Increasing **N** has the effect of increasing the order of the zeros in the frequency response. This, in turn, increases the attenuation at frequencies in the locality of the zero. This effect is clearly illustrated in this figure where we see increasing attenuation of the filter sidelobes as **N** is increased.

[9] This slide is a schematic representation of the CIC core. The CIC filter employs a data-flow style interface for supplying input samples to the Core and for reading the filter output port. ND (New Data), RFD (Ready For Data) and RDY (Ready) are used to coordinate I/O operations. The Core output status signal RFD signals to the system that the filter is ready for data. RFD is active high. Asserting ND high indicates to the Core the availability of a new input sample on the DIN port. ND is very similar in functionality to the clock enable signal found on many VLSI (very large scale integrated-circuit) devices. The RDY output signal indicates that a new filter output sample is available on the DOUT port.

[10] Simulation has been spent with following parameters: **M**=1, **N**=4, **R**=4.

[11] The main formulas about gain output signal and bit growth have been proved and **[12]** simulation of sinus signal has been spent. We seen what the filter works not only on check of theoretical formulas, but also with the real digitized sinusoidal signal. Sinusoidal signal was been repaired even after decimation.

[13] On this slide shown measurement frequency response of designed filter and **[14]** main characteristics has been received.

[15] A CIC filter is typically used in applications where the system sample rate is much larger than the bandwidth occupied by the signal. They are commonly used to build

Digital Down Converters (DDCs) and Digital Up Converters (DUCs). Some applications that use the CIC filter include software designed radios, cable modems, satellite receivers, 3G base stations, and radar systems.

Lattice provides a widely parameterizable CIC filter that supports multiple channels with run-time programmable rates and differential delay parameters.