REGULARITIES OF POWER CONSUMPTION IN QUASIADIABATIC LOGIC GATES

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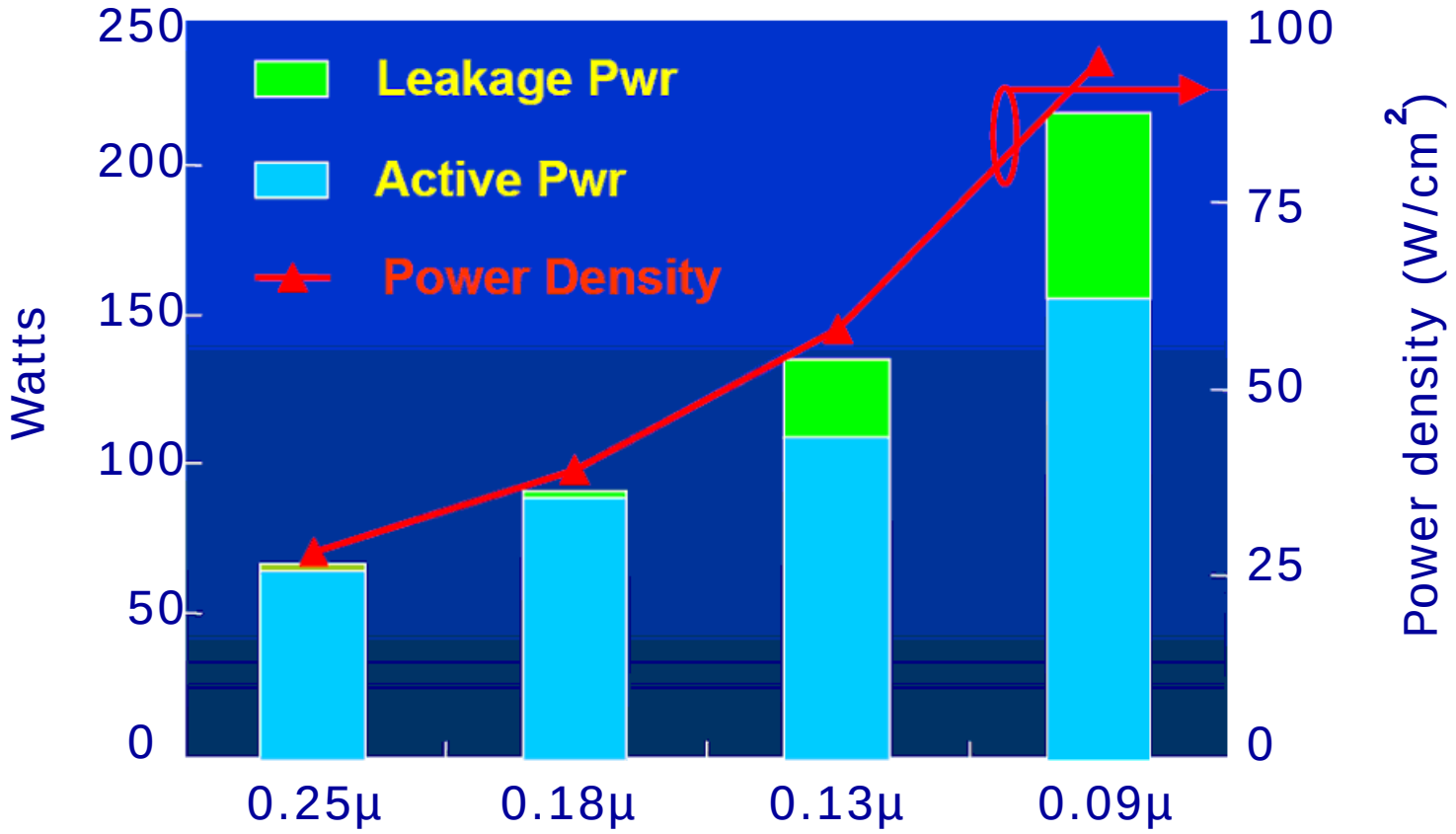
OUTLINE

- *POWER DENSITY TREND*
- *TRADTIONAL WAY TO REDUCE POWER CONSUMPTION*
- *ACTIVE POWER REDUCTION*
- *PERSPICTIVE VARIANTS OF ADIABATIC STATIC LOGIC*
- *QUASIADIABATIC STATIC LOGIC GATES FEATURES*
- *PERSPECTIVE VARIANTS OF ADIABATIC DYNAMIC LOGIC*
- *RESULTS OF SIMULATION*

POWER DENSITY TREND



TRADTIONAL WAY TO REDUCE POWER CONSUMPTION

$$P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{leakage} =$$
$$\alpha_{0->1} C_L \bullet V_{dd}^2 \bullet f_{clk} + I_{sc} \bullet V_{dd} + I_{leakage} \bullet V_{dd}$$

Algoritmical	Logical	Circuits topology	Technology process
Reduce operation per cycle	Boolean function	Type of circuits topology Dynamic logic Static logic, Clock gating Sleep transistors	Leakage (Isolation,SOI) Threshold voltage
Reduce switching activity	Logical basis	MOS, CMOS, BJT, BiCMOS, SiGe	Subthreshold current, Tunneling

ACTIVE POWER REDUCTION

Reduce switched capacitance:
- Minimize loading from diffusion, ware, gate
- Use more efficient layout techniques

Technology scaling:
- Dynamic voltage scaling
- Supply voltage scaling is slowing down
- Thresholds don't scale

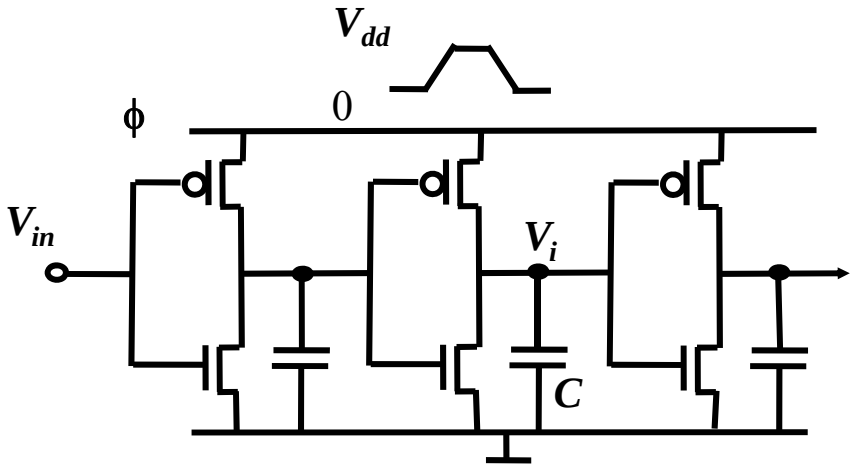
$$P = \alpha C_L V^2 f_{CLK}$$

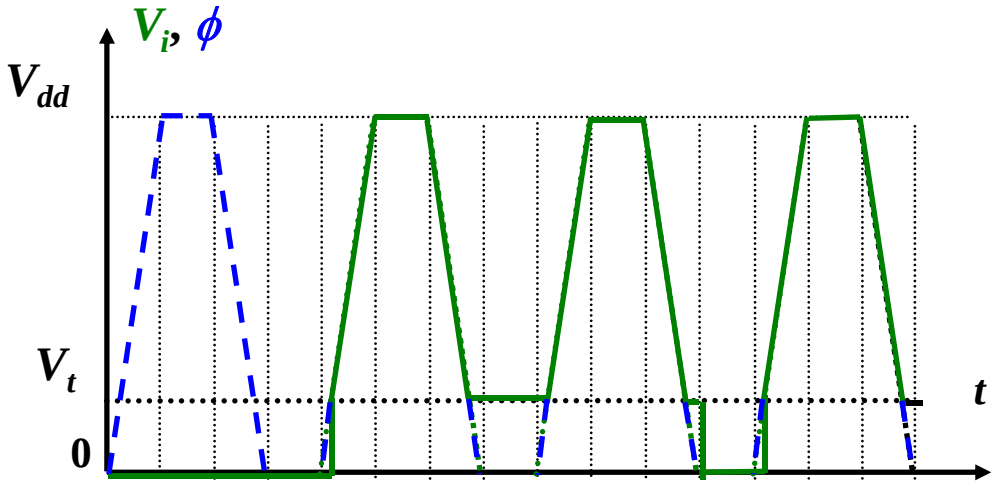
Reduce switching activity:
- Conditional execution
- Conditional clocking
- Conditional precharge
- Turn off inactive blocks

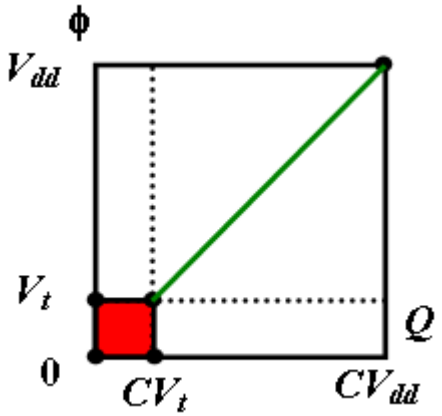
Reduce clock frequency:
- Use parallelism
- Less pipeline stages
- Use double-edge flip-flops

PERSPICTIVE VARIANTS OF ADIABATIC STATIC LOGIC

1n-1p

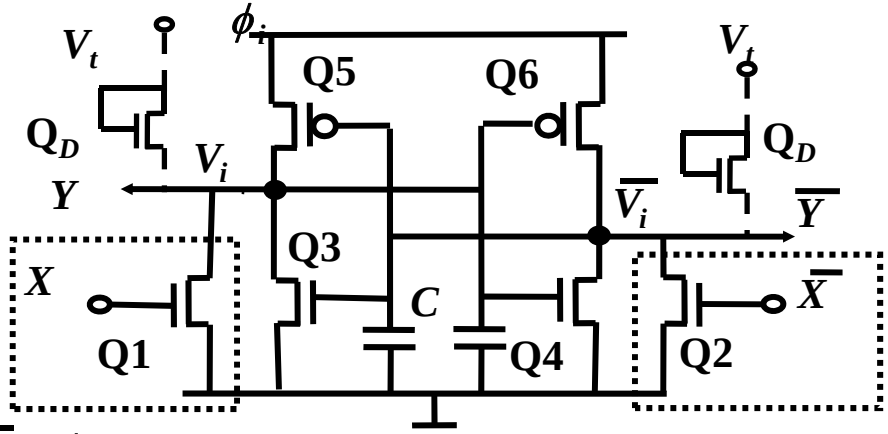


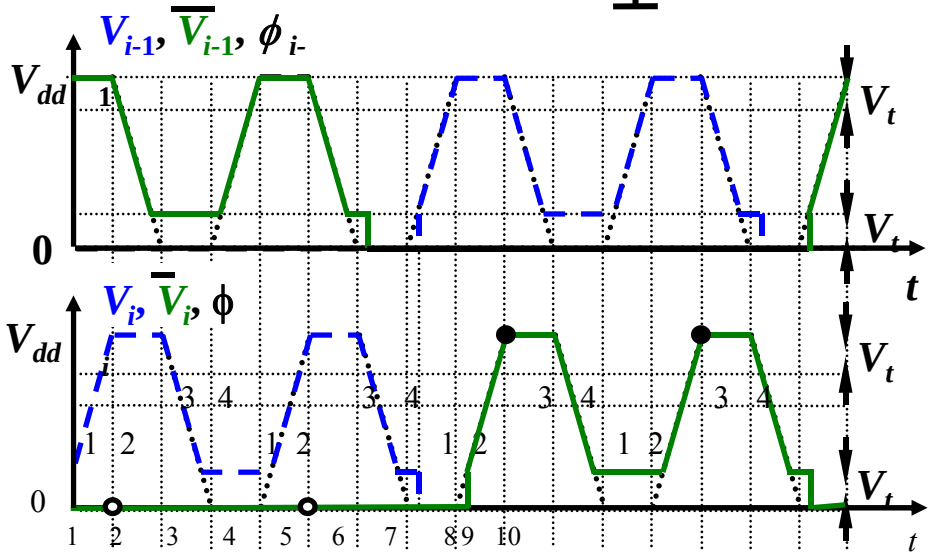




PERSPICTIVE VARIANTS OF ADIABATIC STATIC LOGIC

2n2n-2p



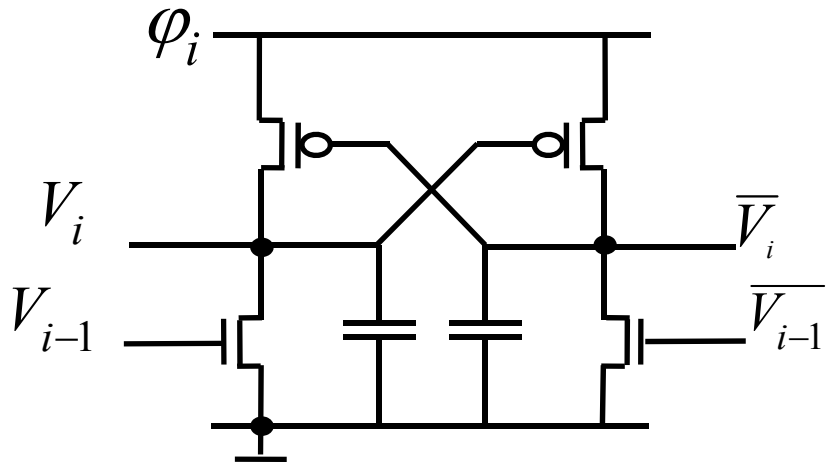


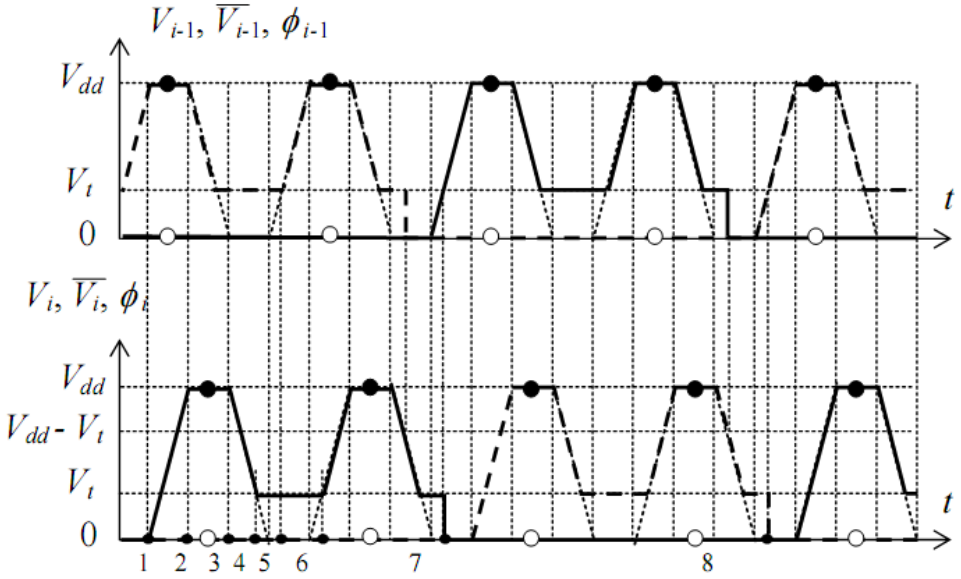
QUASIADIABATIC STATIC LOGIC GATES FEATURES

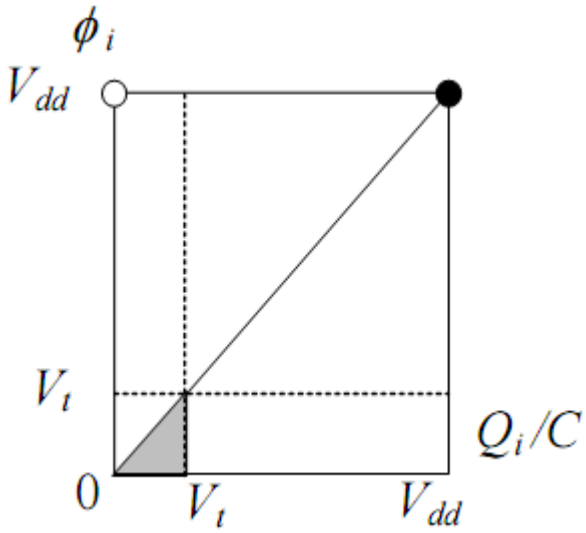
Main features	CMOS	1n1p	2n-2n2p
Degree of adiabatic	0	2	2
pipeline	No	No	Yes
Reliability	Yes	Yes	No
Inverse signal processing	No	No	Yes
MOS q-ty in N input gates	2N	2N	2N+4
Q-ty of power supply phases	0	1	4
Q-ty of power rails	2	2	5
Other req.	—	—	—

PERSPECTIVE VARIANTS OF ADIABATIC DYNAMIC LOGIC

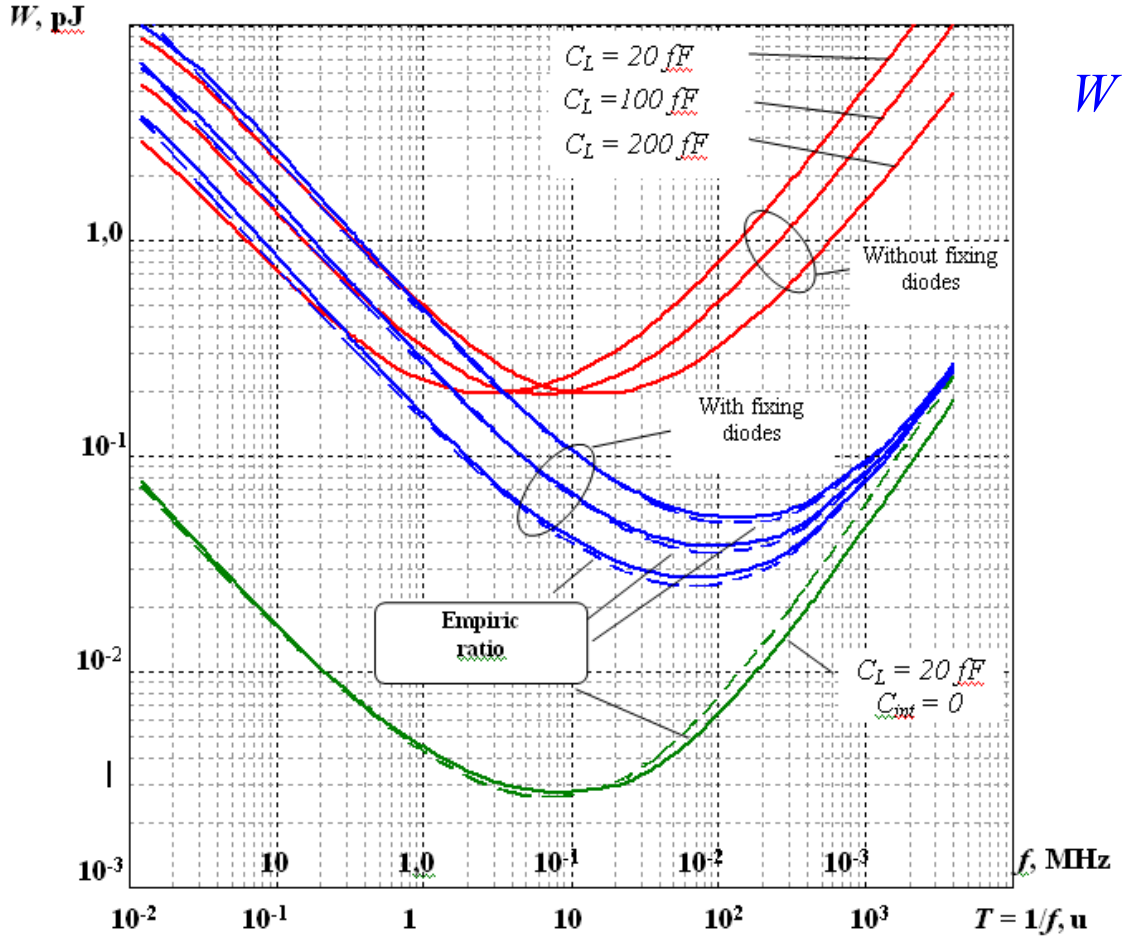
ECRL







RESULTS OF 2n2n-2p LOGIC SIMULATION



$$W = 4W_0 = \int_{4T} \phi_i(t) I_i(t) dt$$

I_i -the current consumed by i-gate

C_L -load capacity

C_{int} -internal transistor capacities

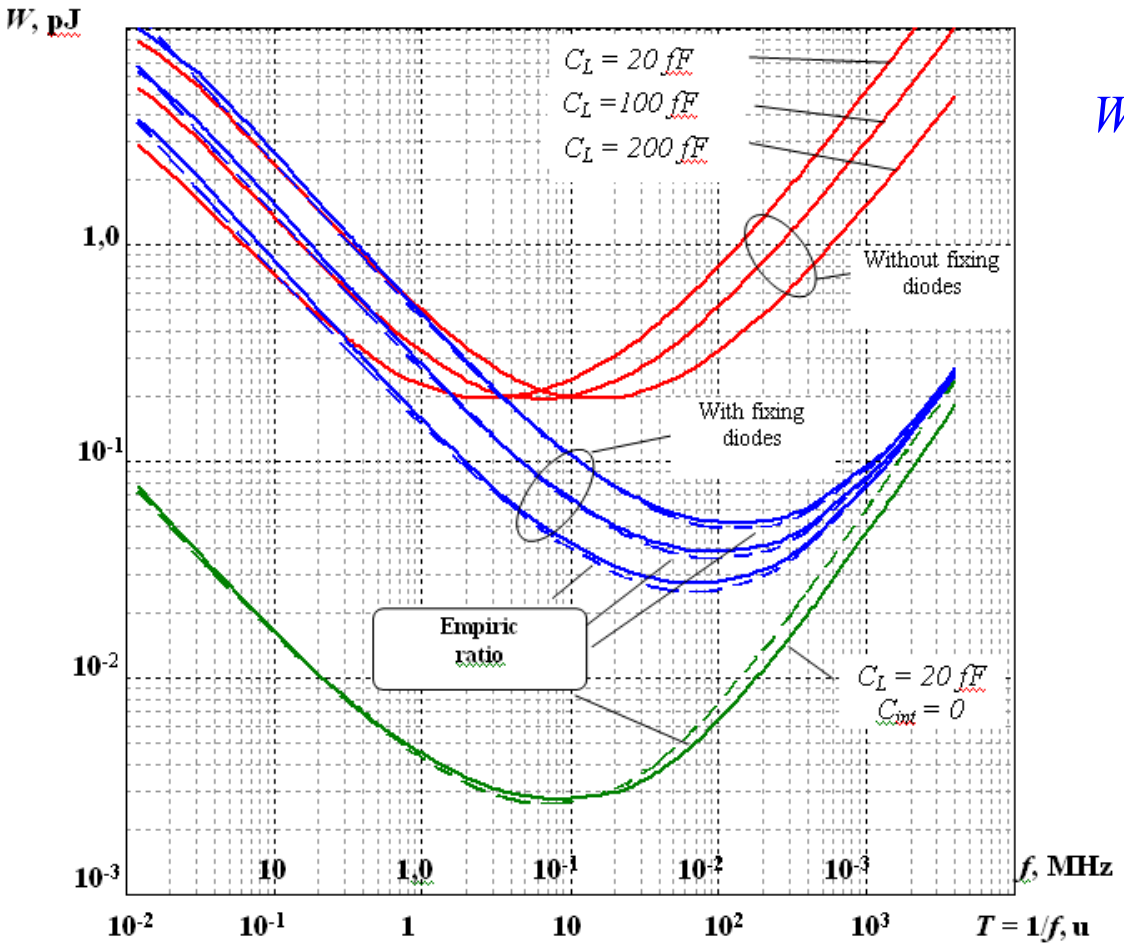
$\alpha = 0.75$

$R_{ef} = 3.9\,кОм$

$C_{\text{int}} = 170\,фФ$

$P_0 = 11,4\,\text{пВт}$

RESULTS OF ECRL LOGIC SIMULATION



$$W = 4W_0 = \int_{4T} \phi_i(t) I_i(t) dt$$

I_i -the current consumed by i-gate

C_L -load capacity

C_{int} -internal transistor capacities

$\alpha = 0.73$

$R_{ef} = 3.02\,\text{кОм}$

$C_{\text{int}} = 140\,\text{фФ}$

$P_0 = 10\,\text{пВт}$

CONCLUSION

- *The established laws allow to choose the compromise between power consumption and speed, optimize power characteristics of base gates.*
- *It's also allowed to predict their improvement at quality of technology*

THANK YOU!