CMOS Model's FLAG Control System

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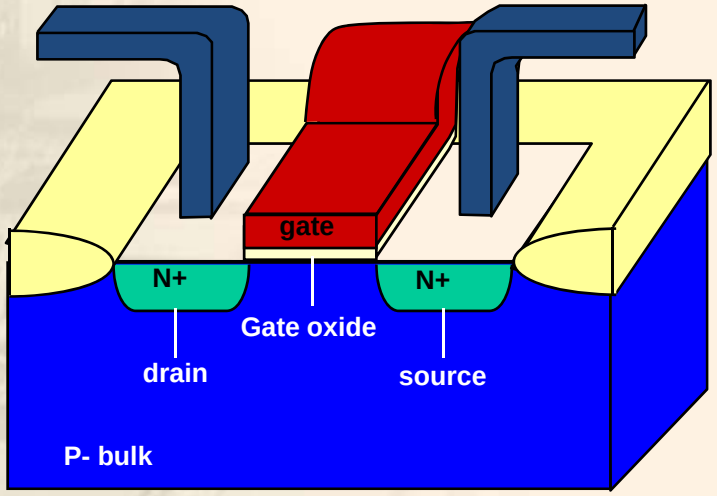
Contest

- Evolution of CMOS transistors models
- Results of CMOS transistors models evolution
- Drawbacks of existing approaches
- Proposed approaches for model speed and accuracy increase
- Target function definition for CMOS model speed and accuracy increase
- Proposed flow for model speed and accuracy increase
- Example Accuracy and speed increase flow application
- Accuracy and speed increase flow application results
- CMOS model speed and accuracy increase software structure and functionality
- FLAG software graphical interface
- FLAG efficiency estimation

CMOS transistors models evolution (1)



BSIM1

$$V_{th} = \begin{cases} V_{Thideal.} = V_{th0} = V_{Fb} + \Phi_s + K_1 \cdot \sqrt{\Phi_s} \\ \Phi_s = 2 \cdot V_{tm0} \ln\left(\frac{N_{ch}}{n_{i0}}\right), \text{at } T = T_{nom} \\ V_{tm0} = \frac{K_B \cdot T_{nom}}{q} \end{cases}$$

CMOS transistors models evolution (2)

BSIM4

$$V_{th} = V_{thideal} + \Delta V_{th(1)} + \Delta V_{th(2)} + \Delta V_{th.(3)} + \Delta V_{th.(4)} + \Delta V_{th.(5)} + \Delta V_{th.(6)}$$

$$\Delta V_{th(1)} = K_1 \cdot \frac{T_{ox}}{T_{oxm}} \cdot \sqrt{\Phi_s - V_{bseff}} - K_2 \cdot \frac{T_{ox}}{T_{oxm}} \cdot V_{bseff}$$

$$\Delta V_{th(2)} = K_1 \cdot \frac{T_{\hat{u}x}}{T_{\hat{u}xm}} \cdot \sqrt{1 + N \cdot L_{eff} / L_{eff}} \cdot \sqrt{\Phi_s}$$

$$\Delta V_{th}(4) = D_{VTO} \left(e^{\left(-D_{VT1} \frac{W_{eff} L_{eff}}{2 L_{tw}} \right)} + 2 e^{\left(-D_{VT1} \frac{W_{eff} L_{eff}}{L_{tw}} \right)} \right) \cdot \left(V_{bi} - \varphi_s \right)$$

$$\Delta V_{th}(6) = \left(e^{\left(D_{VT1} \cdot \frac{L_{eff}}{2 * L_{t0}} \right)} + 2 \cdot e^{\left(D_{VT1} \cdot \frac{L_{eff}}{L_{t0}} \right)} \right) \cdot \left(E_{ta0} + E_{tab} \cdot V_{bseff} \right)$$

$$l_{t0} = \sqrt{\frac{\varepsilon_{si} \cdot T_{ox} \cdot X_{dep}}{\varepsilon_{sio2}}}$$

$$Vbseff = V_{bc} + 0.5 \cdot \left[V_{bs} - V_{bc} - \delta_1 + \sqrt{\left(V_{bs} - V_{bc} - \delta_1 \right)^2 - 4 \cdot \delta_1 \cdot V_{bc}} \right]$$

$$K_1 = \gamma_2 - 2 \cdot K_2 \cdot \sqrt{\Phi_s - V_{bm.}}$$

$$K_2 = \frac{(\gamma_1 - \gamma_2) \cdot (\sqrt{\Phi_s - V_{bx.}} - \sqrt{\Phi_s})}{2\sqrt{\Phi_s} \cdot (\sqrt{\Phi_s - V_{bx.}} - \sqrt{\Phi_s}) + V_{bx.}}$$

$$\gamma_1 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{ch}}}{C_{\hat{u}x}}$$

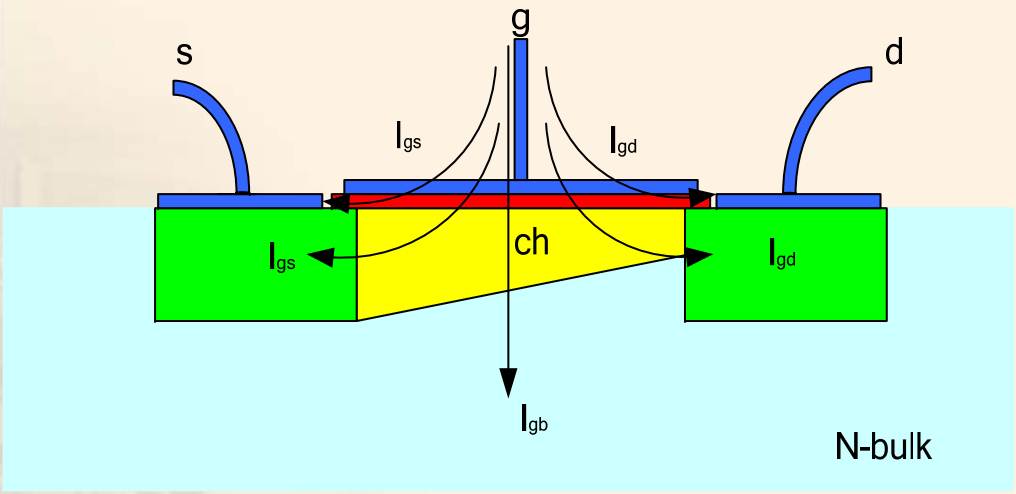
$$\gamma_2 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{ch.}}}{C_{\hat{u}x}}$$

$$X_t = \Phi_s - \frac{q \cdot N_{ch} \cdot X_t^2}{2 \cdot \varepsilon_{si}}$$

$$V_{bc} = 0.9 \cdot \Phi_s + \frac{K_1^2}{4 * K_2^2}$$

CMOS transistors models evolution (3)

BSIM5 - new physical effects



$$|I| = |U| \cdot \omega \cdot C$$

$$C_{db} = C_{s.b} + C_{d.b} + C_{h.b}$$

$$C_s = C_s = \frac{1}{2} \cdot W \cdot L \cdot C_{ox}$$

$$C_{ch} = \frac{2}{3} \cdot W \cdot L \cdot C_{ox}$$

$$C_{Ñá.Ñ^3} = W \cdot L \cdot C_{ûùëÇ^1}$$

$$C_{3ï} = C_{3ñ} = 0$$

$$I_h = W_{eff} \cdot L_{eff} \cdot A \left(\frac{TOXREF}{TOXE} \right)^{NTOX} \cdot \frac{1}{TOVE^2} \cdot V_{th} \cdot$$

$$\cdot V_{aux1} \cdot \exp(-B \cdot TOXE \cdot (AIGBACC - BIGBACC \cdot V_{oxacc}) \cdot$$

$$\cdot (1 + CIGBACC \cdot V_{oxacc}))$$

$$I_h = W_{¿ýý} \cdot L_{¿ýý} \cdot C \cdot \left(\frac{TOXREF}{TOXE} \right)^{NTOX} \cdot \frac{1}{TOVE^2} \cdot V_{th} \cdot$$

$$\cdot V_{aux2} \cdot \exp(-D \cdot TOXE \cdot (AIGBINV - BIGBINV \cdot V_{oxdep}) \cdot$$

$$\cdot (1 + CIGB \cdot ACCINV \cdot V_{oxdep}))$$

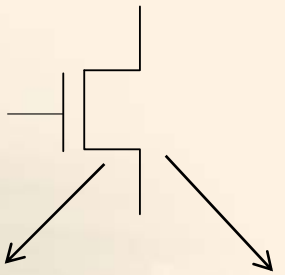
$$I_h = W_{¿ýý} \cdot L_{¿ýý} \cdot E \cdot \left(\frac{TOXREF}{TOXE} \right)^{NTOX} \cdot \frac{1}{TOVE^2} \cdot V_{gse} \cdot NIGC \cdot$$

$$\cdot V_t \cdot \log \left(1 + \exp \left(\frac{V_{gse} - VTH0}{NIGC * V_t} \right) \right) \cdot$$

$$\cdot \exp(-F \cdot TOXE \cdot (AIGC - BIGC \cdot V_{oxde}) \cdot$$

$$\cdot (1 + CIGB \cdot ACCINV \cdot V_{ûxde}))$$

Results of CMOS transistors models evolution



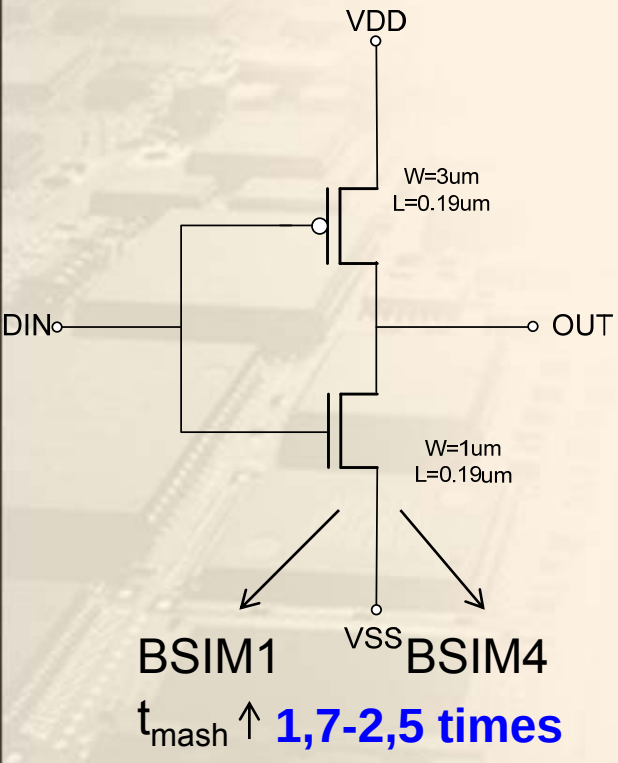
BSIM1 BSIM4

t_{mash} ↑**1,5-2 times**

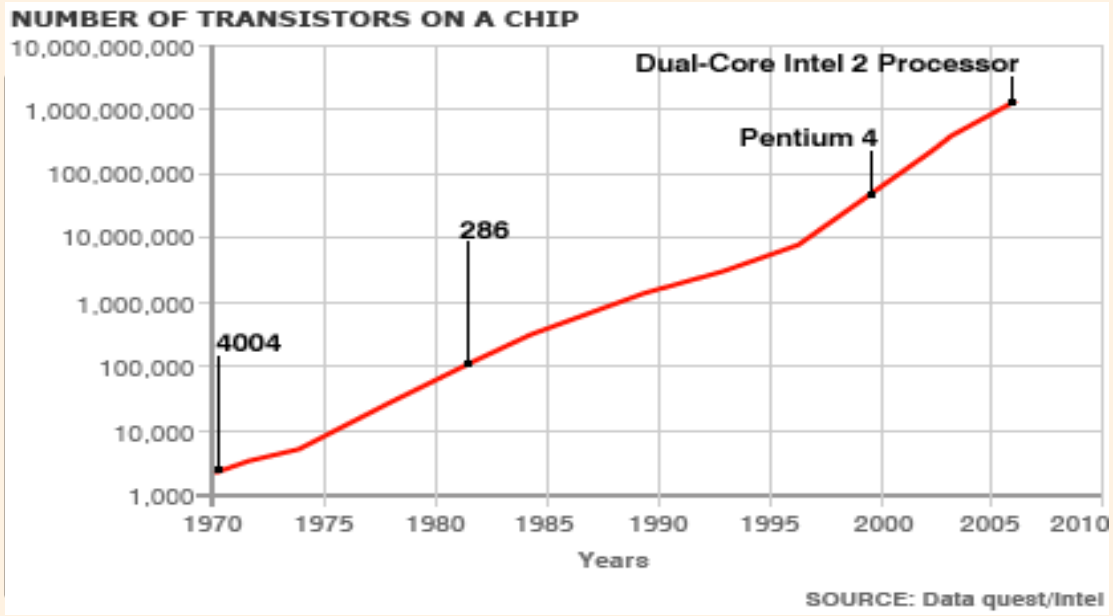
New physical effect → Analysis complexity → Model → Equation Complication

Parameters number growth

IC elements number growth



t_{mash} ↑ **1,7-2,5 times**

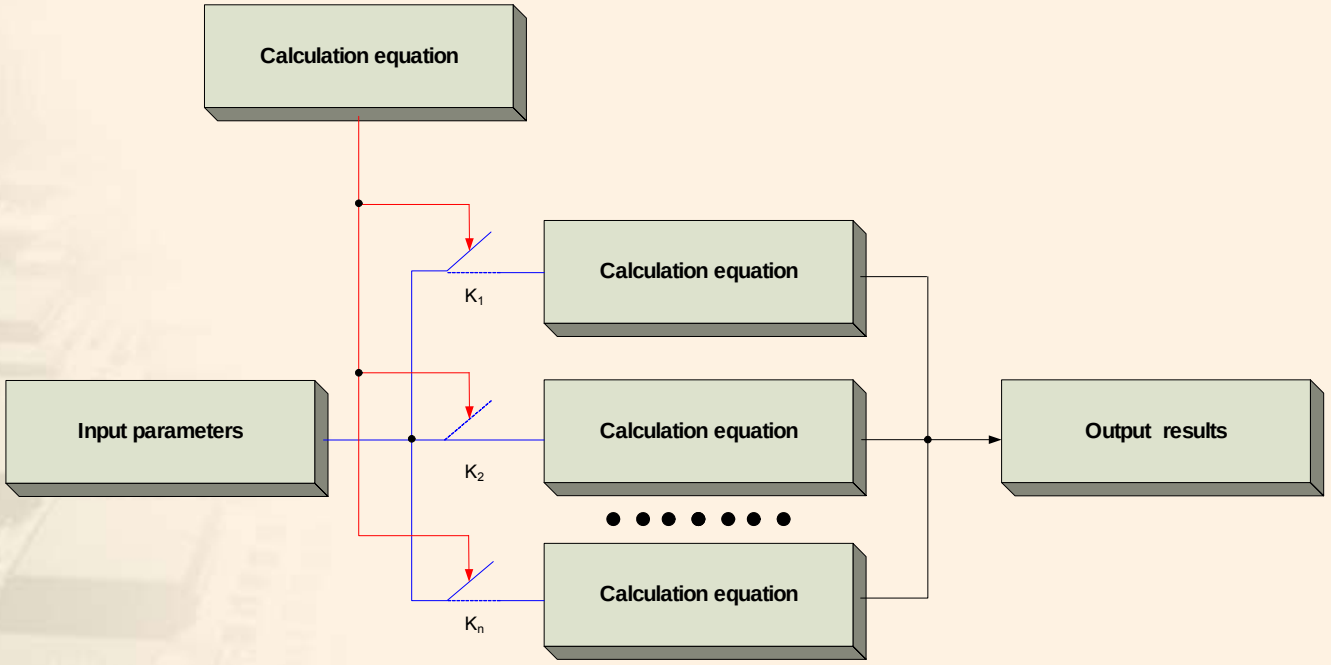


Need in increase of model speed and accuracy

Proposed approaches for model speed and accuracy increase (1)

1. Trade-off between number of operations and achieved accuracy in avery computational case

Computational gates application flow



$$\mu_{¿ýý} = \frac{\mu_0}{1+U_a\cdot((V_{gs}+V_{bseff})/T_{ox})+U_b((V_{gs}+V_{bseff})/T_{ox})^2+U_c\cdot V_{bs}}$$

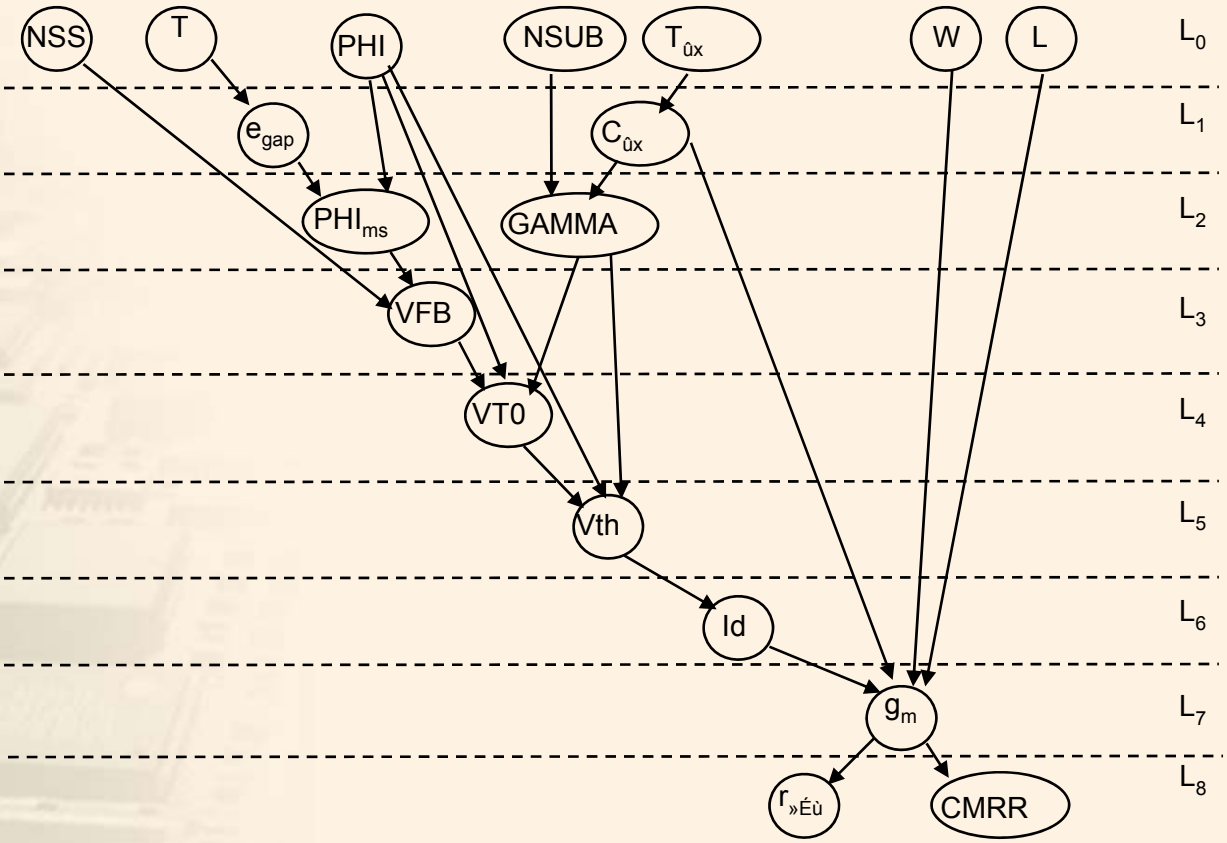
mobmod=1

$$\mu_{¿ýý} = \frac{\mu_1}{1+(U_a+U_c\cdot V_{bseff})\cdot((V_{gsteff}+2\cdot V_{th})/Tox)+U_b((V_{gsteff}+V_{th})/Tox)^2}$$

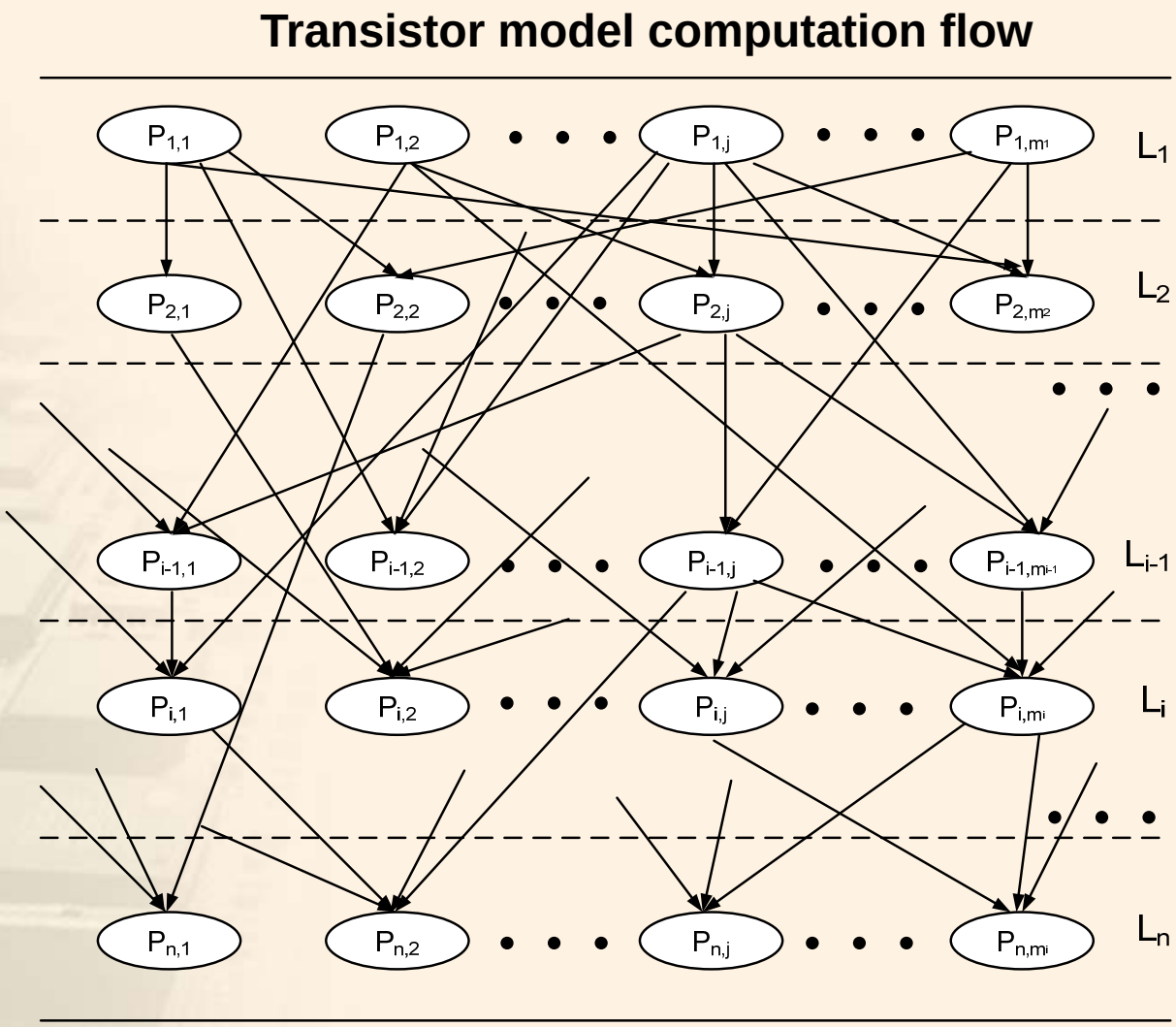
mobmod=2

Proposed approaches for model speed and accuracy increase (2)

2. Elimination of information lack and excess during calculations

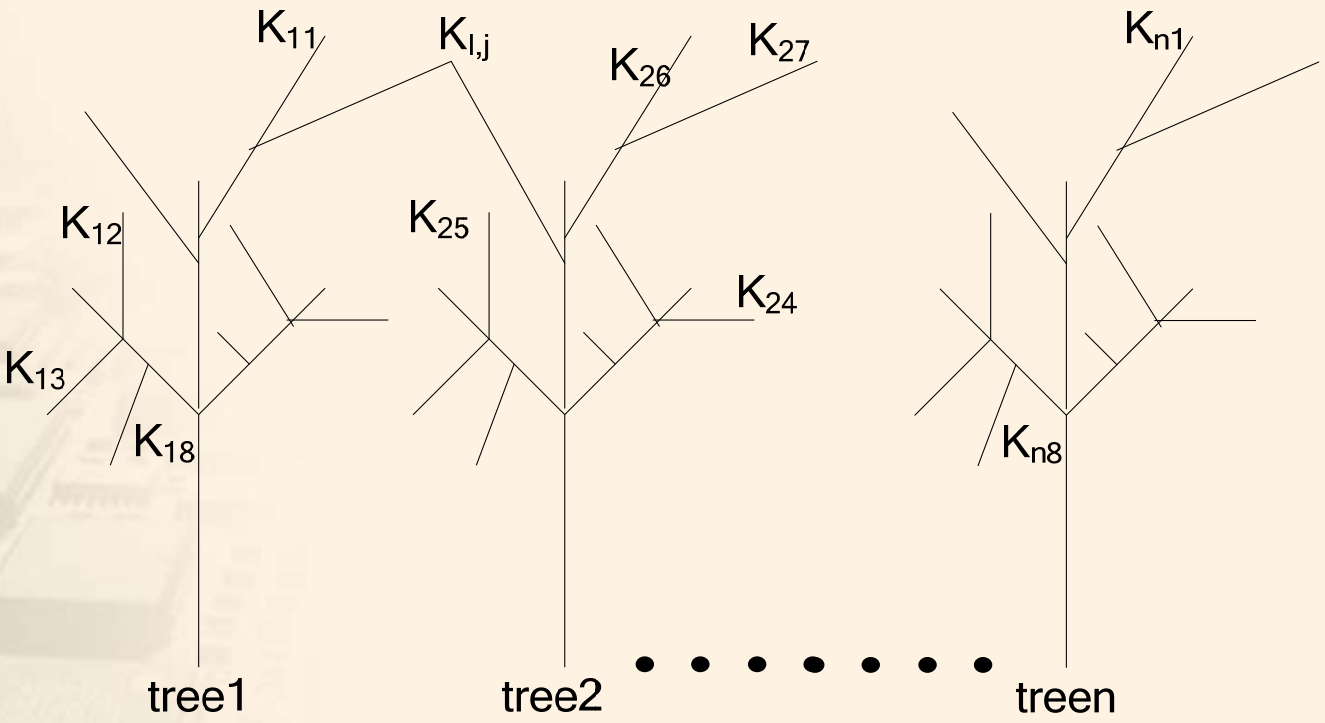


Proposed approaches for model speed and accuracy increase (3)



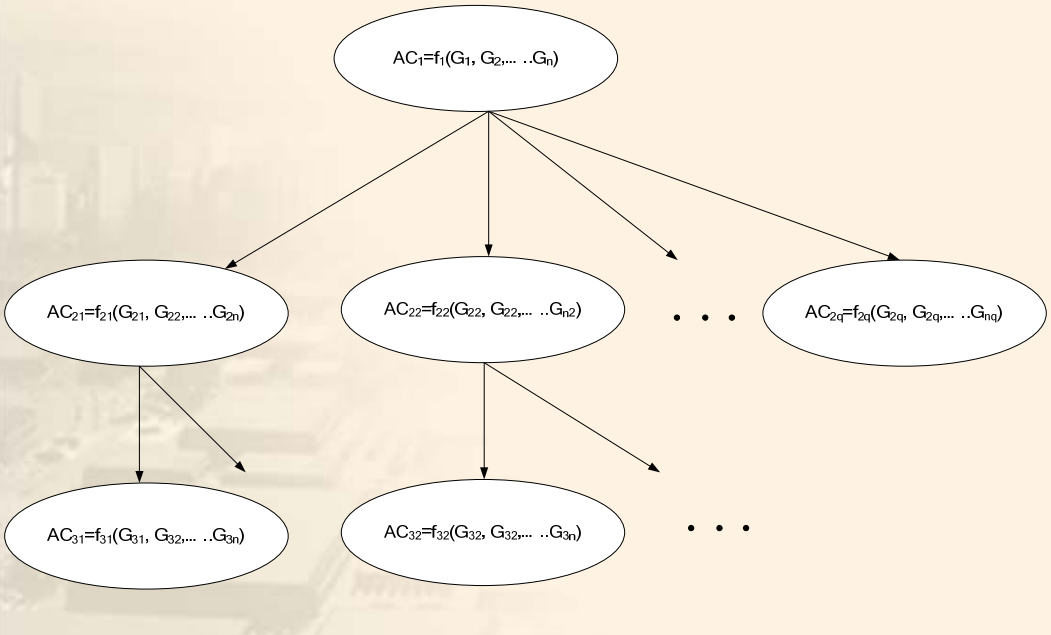
Proposed approaches for model speed and accuracy increase (4)

Trees of computational gates



Proposed approaches for model speed and accuracy increase

3. Different accuracy for transitions depending on demands occurring during current computational situation



Hierarchy of adaptation criteria used in CMOS transistor's model

4. Model universality: independency from modelin circuit, technological process, circuit base, etc.

5. CMOS transistor compatibility with other electrical elements' models (diodes, resistors, etc): no need in recalculations during modeling with such models

Target function definition for CMOS model speed and accuracy increase

Target function

$$E_{mach} \rightarrow \min$$

Limitation

$$\Delta_{calc} < \Delta_{alow} \quad \& \quad \varepsilon_{calc} < \varepsilon_{alow}$$

$$a_i \le P_i \le b_i, i=1,2...,S$$

$$\Delta_{calc} = \vec{Y}_{calc} - \vec{Y}_{real}$$

$$\varepsilon_{calc} = \frac{\vec{Y}_{calc} - \vec{Y}_{real}}{\vec{Y}_{calc}}$$

$$\vec{Y}_{calc} = F(AC_{ij} = f(G_{ij}))_{i=1,2,...,t;j=1,2,...,q}$$

$$E_{mach} = \sum_{d=1}^{n} t_{mach} = \Psi(AC_{ij} = f(G_{ij}))_{i=1,2....,t;j=1,2,...,q}$$

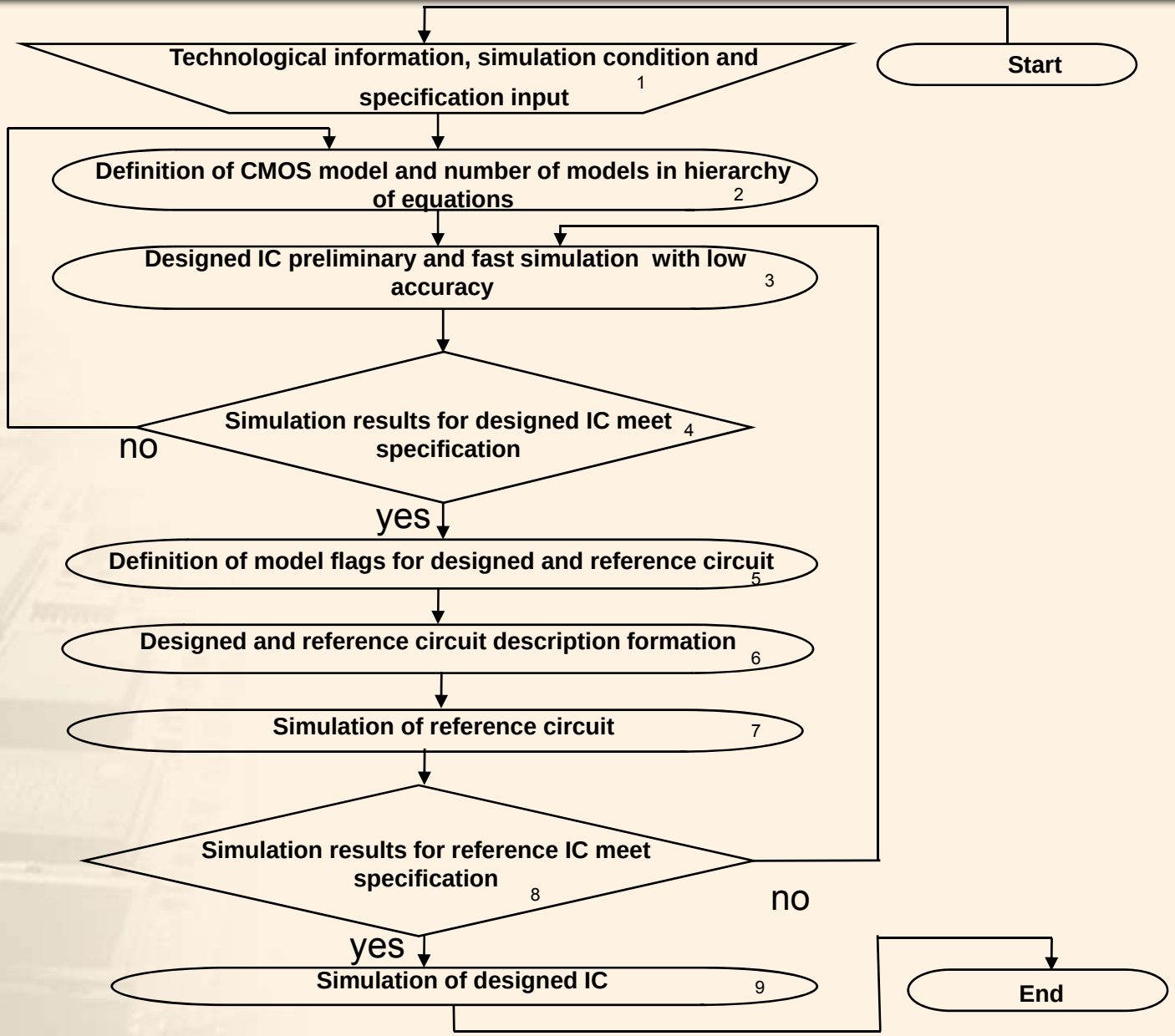
$$F(AC_{ij} = f(G_{ij}))_{i=1,2,...,t;j=1,2,...,q} - \vec{Y}_{real} < \Delta_{alow}$$

$$\frac{F(AC_{ij} = f(G_{ij}))_{i=1,2,...,t;j=1,2,...,q} - \vec{Y}_{çñ³ Ï.}}{\vec{Y}_{real}} < \varepsilon_{alow}$$

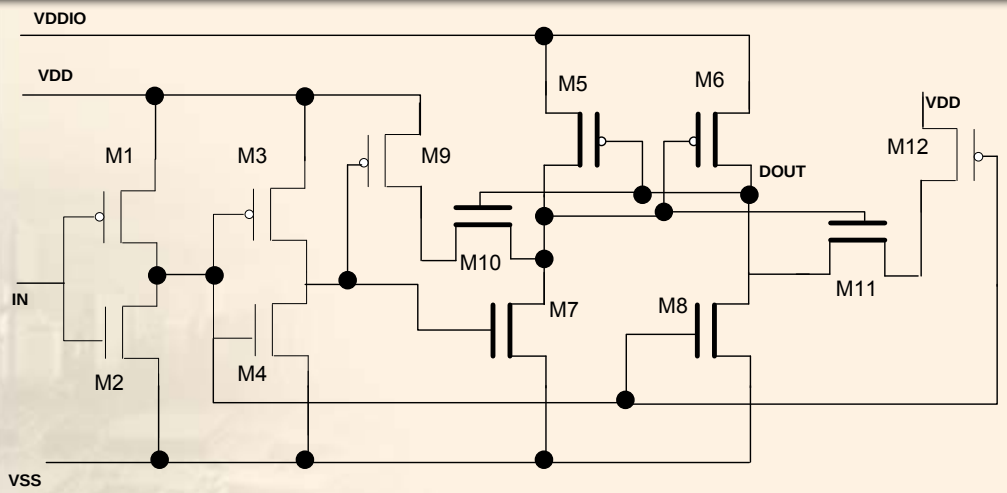
$$a_i \le p_i \le b_i, i=1,2...,S$$

$$E_{mach} = \psi(AC_{ij} = f(G_{ij}))_{i=1,2....,t;j=1,2,...,q} \rightarrow \min$$

Proposed flow for model speed and accuracy increase



Example
Accuracy and speed increase flow application (1)



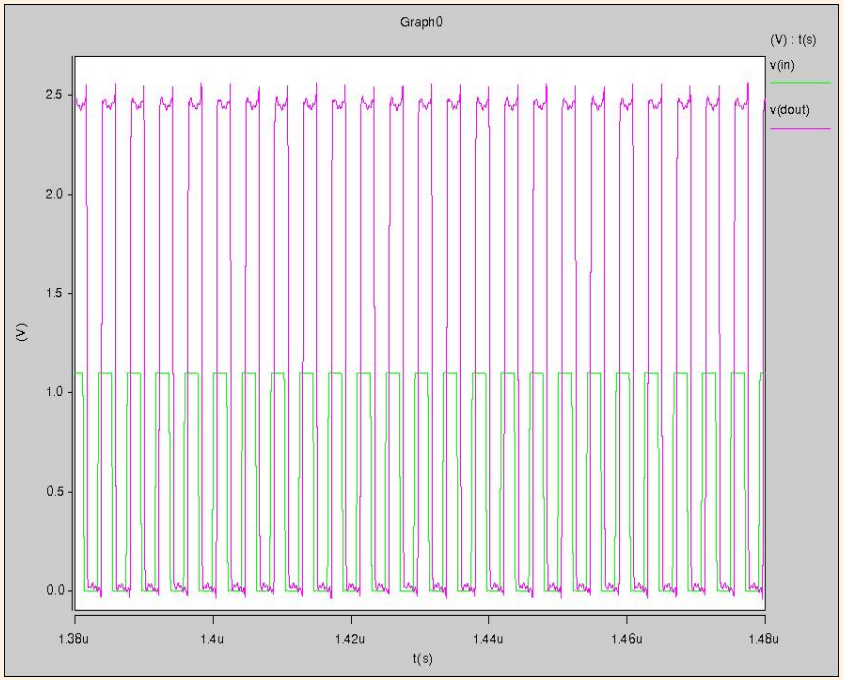
Low to high level shifter

Level shifter operating conditions

Parameters	Typical	Min	Max	Dimension
Core supply (VDD)	1,2	1,08	1,32	V
I/O supply (VDDIO)	2,5	2,25	2,75	V
Clock frequency	240	120	-	MHc
Temperature	25	125	-40	ûC
Power dissipation	10	-	11	uWt

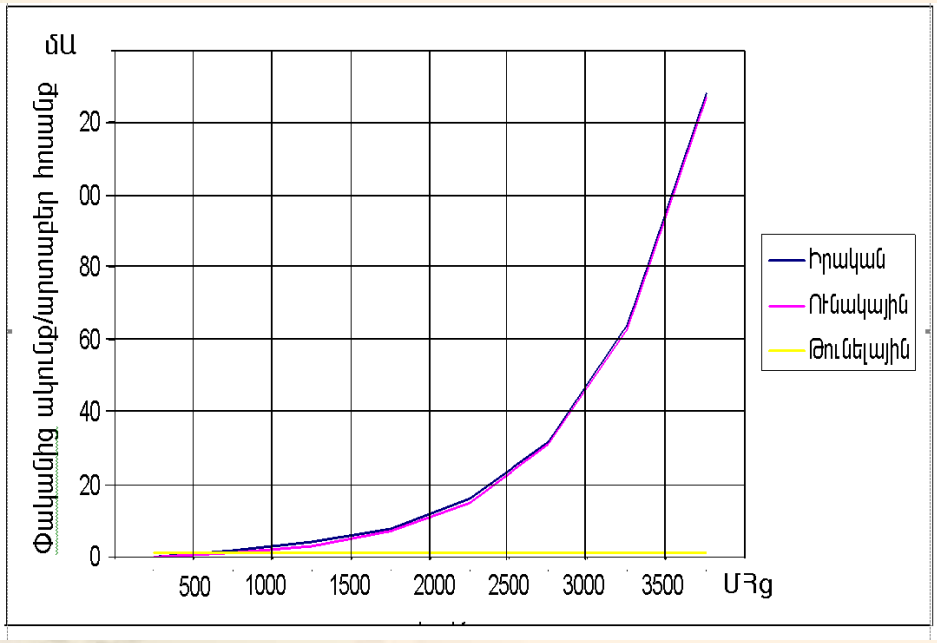
Level shifter specification and technology information

parameters	typical	min	max	Dimension
Simulation time	64	-	70	s
Calculations results accurse	99	97	-	%
Technology	TSMC65	-	-	-
Thick oxide transistor	yes	-	-	-
Thin oxide transistor	yes	-	-	-
Channel length	-	65	-	nm



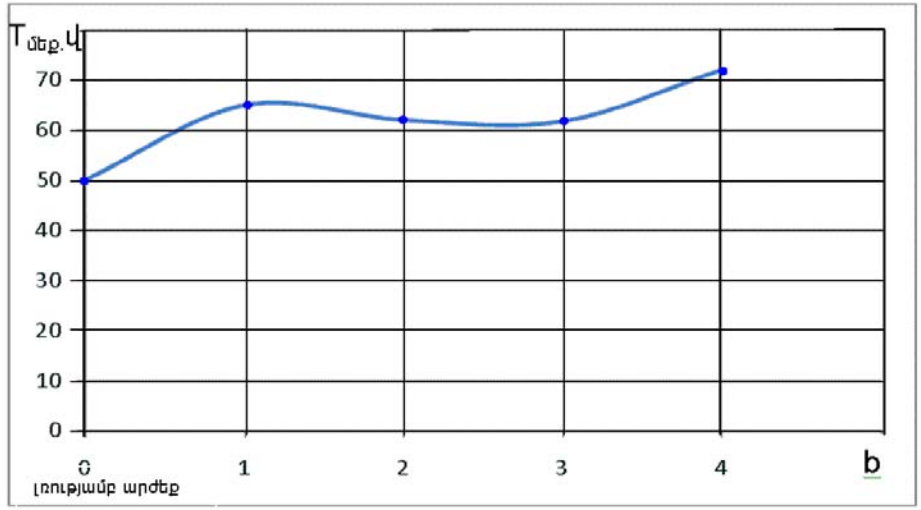
Simplified simulation results

Example
Accuracy and speed increase flow application (3)



Simulation time dependence from number of computational gates for TSMC65

Frequency simulation results for gate capacitive and tunneling currents

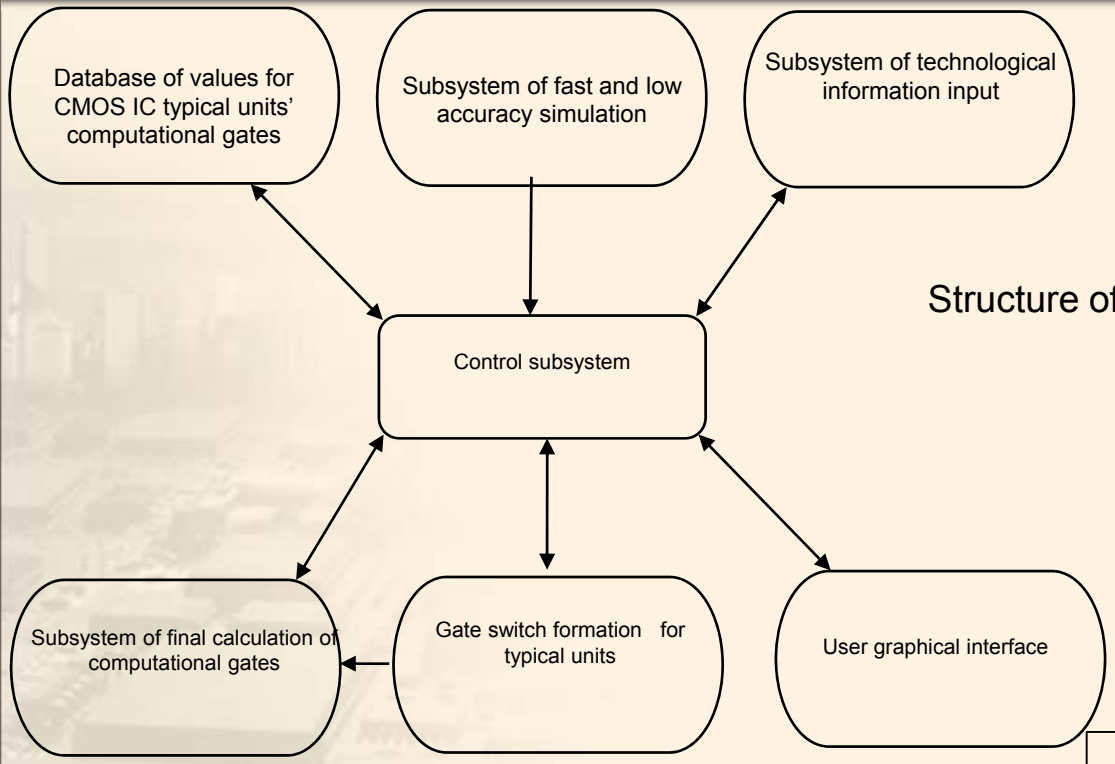


Accuracy and speed increase flow application results

FLAG	BSIM 4.4.0	Gain
Average relative error with this model		
0,0248 %	1,7%	1,67%
Time needed for simulation with this model		
57,14 í	84.97 í	27.83 s/ 47%

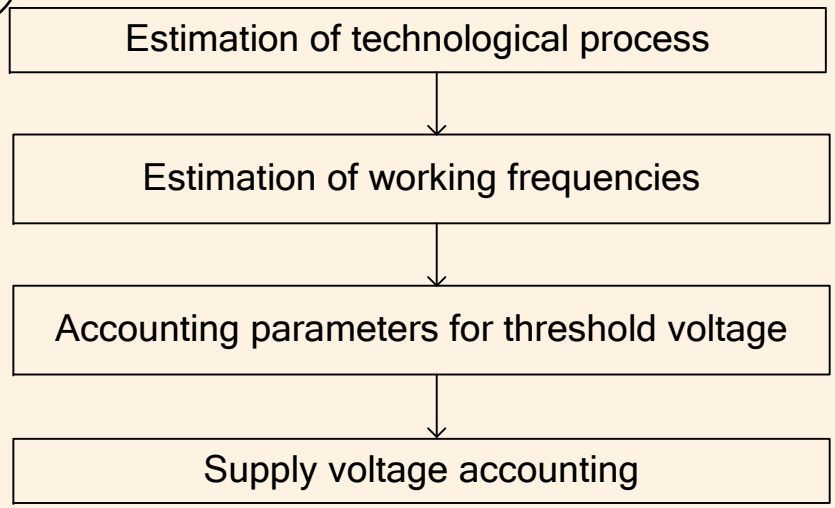
More accurate results need more time

CMOS model speed and accuracy increase software structure and functionality

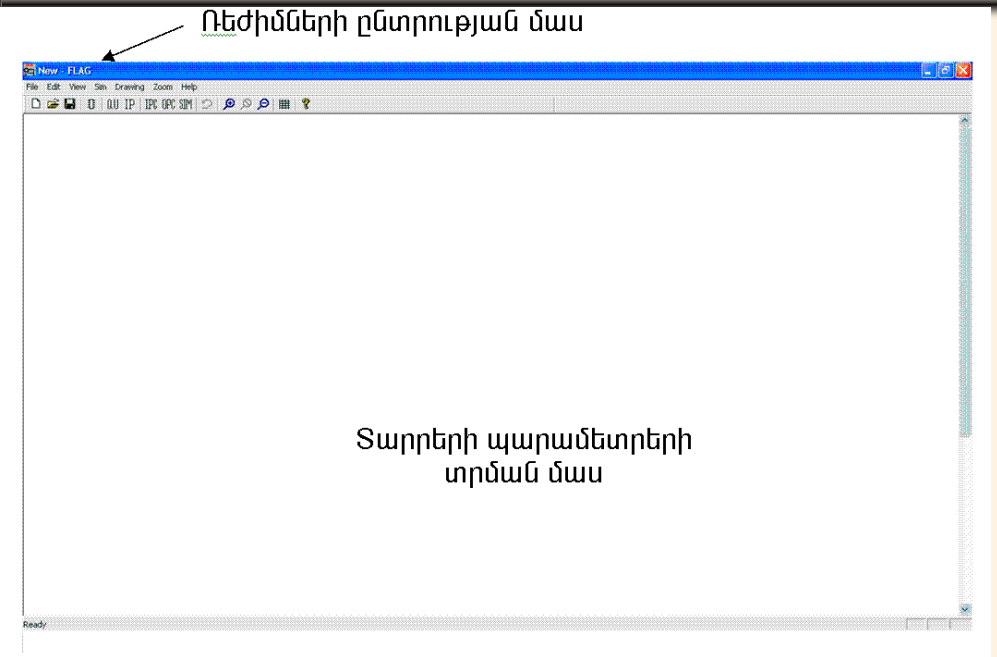


Structure of model accuracy and speed increase FLAG software

Process of calculation equation selection

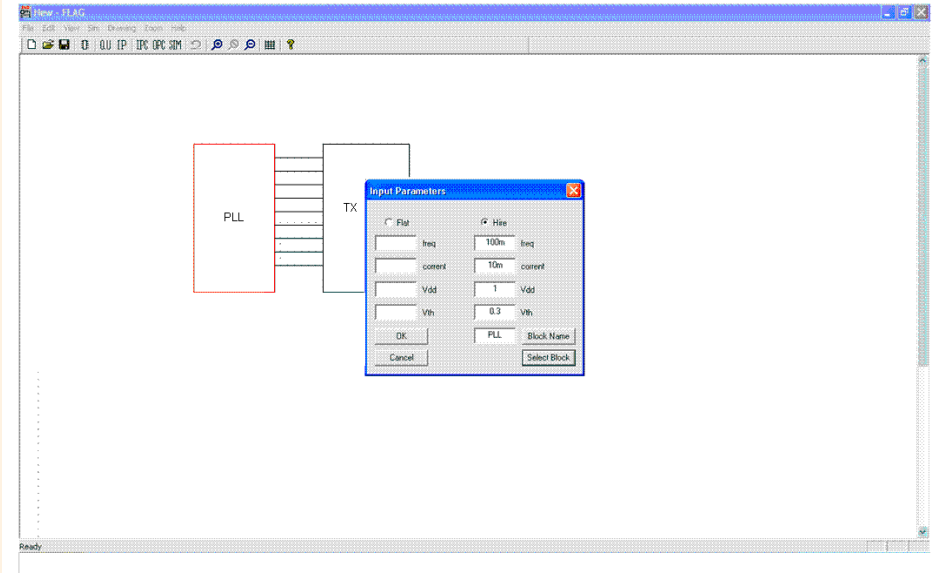


FLAG software graphical interface

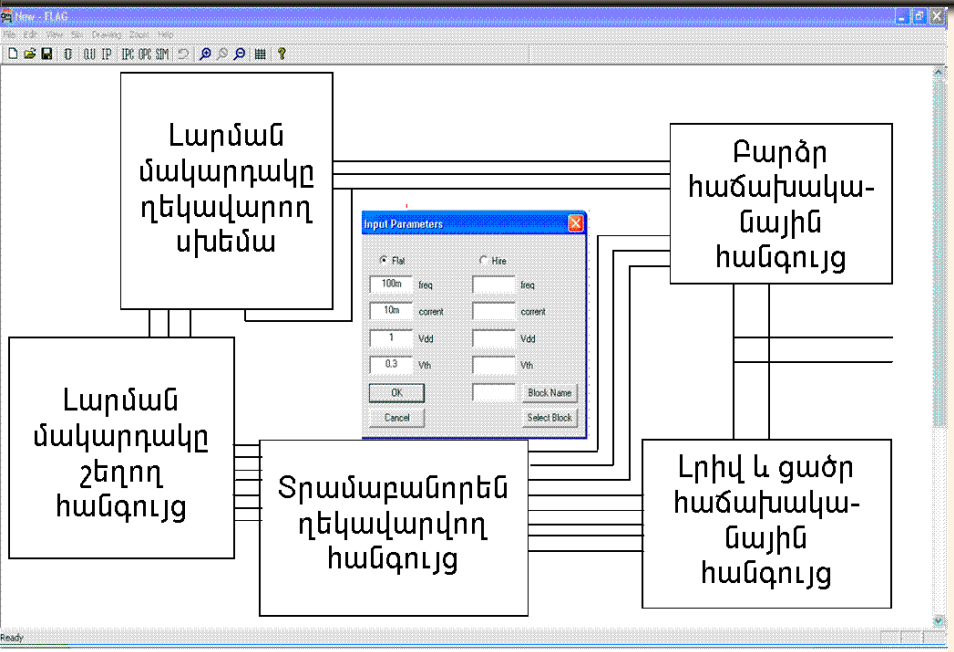


Input of model separate parameter

IC simulation parameter selection



FLAG efficiency estimation (1)

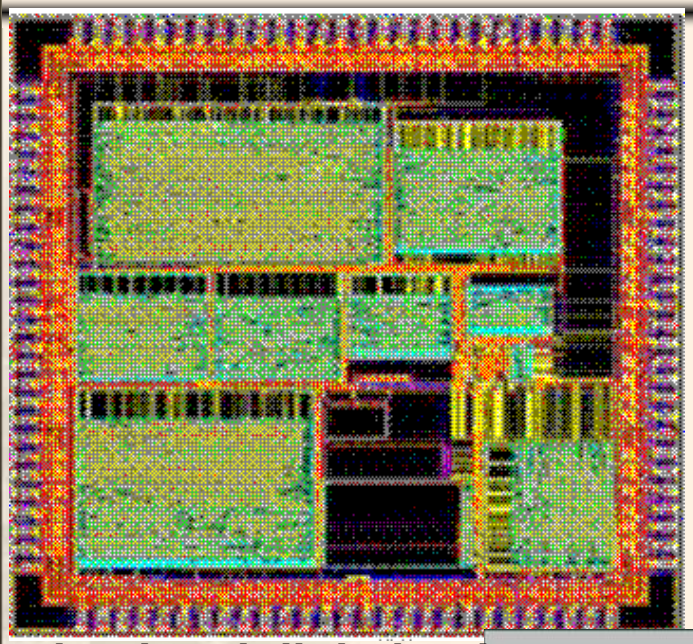


USB TX block-diagram

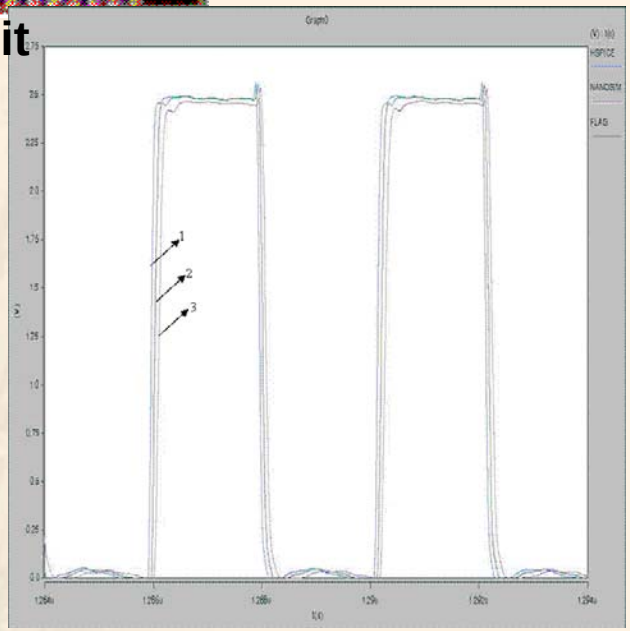
USB TX simulation time comparison

Processing steps	Synopsys	Cadence	FLAG	Comparative gain (%)
				Synopsys/ Cadence
Preliminary model construction	-	-	3,2ñ	-
IC preliminary simulation	-	-	61,21ñ	-
Model switch optimizations	-	-	1,12ñ	
IC simulation time	18,4Å	21,2Ä	6,2Å	61,12%/ 73,4%
IC simulation accuracy	96,1%	96,2%	98,4%	2,3%/2,2%

FLAG efficiency estimation (2)



Simulated digital unit



Processing steps	Synopsys	Cadence	FLAG	Comparative gain (%)
				Synopsys/ Cadence
Preliminary model construction	-	-	30,3min	-
IC preliminary simulation	-	-	10,46h	-
Model switch optimizations	-	-	39min	
IC simulation time	10,6day	10,2day	1,5day	81,1%/ 79,8%
IC simulation accuracy	82,5%	82,2%	96,9%	14,4%/ 14,7%

Digital unit's simulation results
1` Real chip measurements, 2` simulated with FLAG, 3` simulated with Nanosim

Thank you