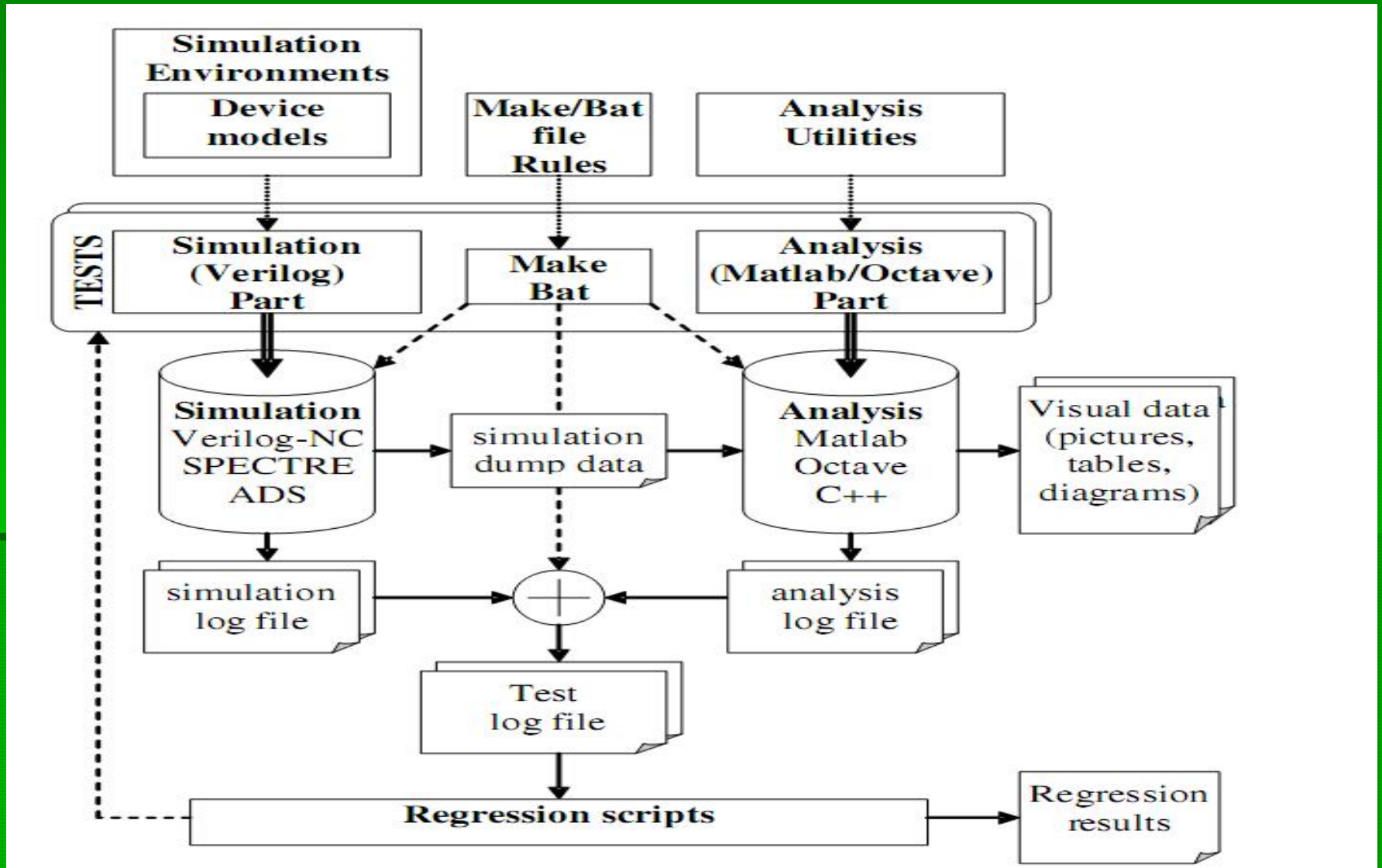
# "Development and optimization tests for detection fabrication faults in mixed-signal circuits".

- Belousov A. V.

# The organisation of a test environment.



# Performing Manufacturing Testing

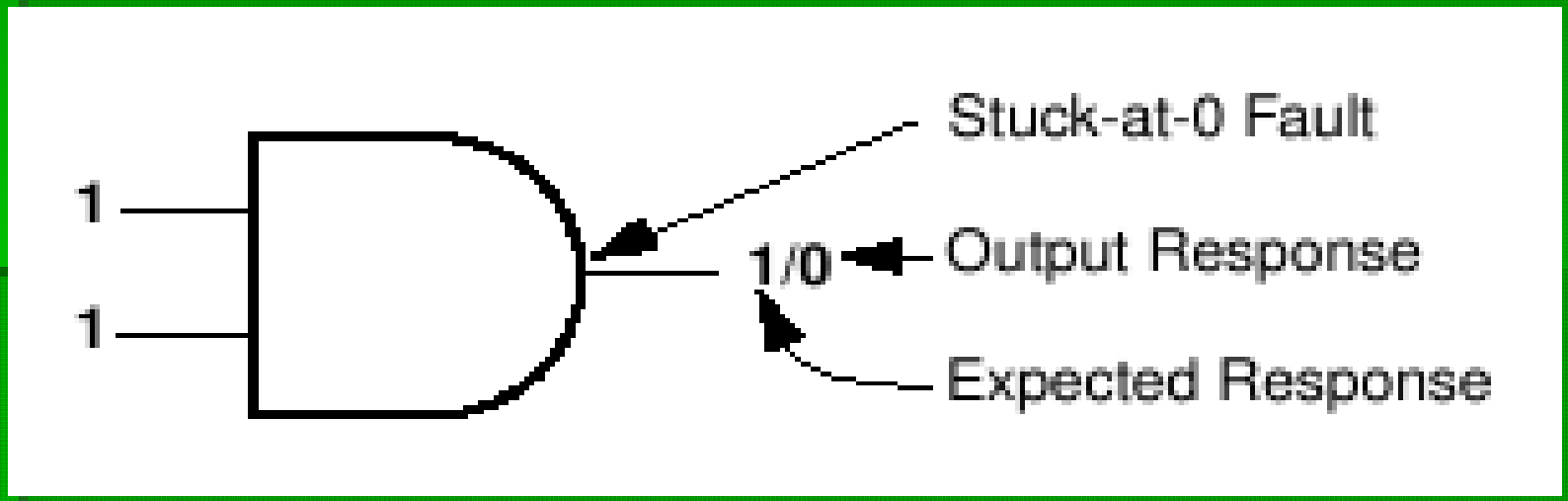
- functional testing verifies that your circuit performs as it was intended to perform.
- manufacturing testing verifies that your circuit does not have manufacturing defects by focusing on circuit structure rather than functional behavior.
- manufacturing defects include problems such as the following:
  - Power or ground shorts
  - Open interconnect on the die caused by dust particles
  - Short-circuited source or drain on the transistor caused by metal spike-through
- manufacturing defects might remain undetected by functional testing yet cause undesirable behavior during circuit operation. )

# Fault Models

- A manufacturing defect has a logical effect on the circuit behavior. An open connection can appear to float either high or low, depending on the technology. A signal shorted to power appears to be permanently high. A signal shorted to ground appears to be permanently low. Many of these manufacturing defects can be represented using the industry-standard stuck-at fault model. Other faults can be modeled using the IDDQ, or quiescent current fault model.

# Stuck-At Fault Models

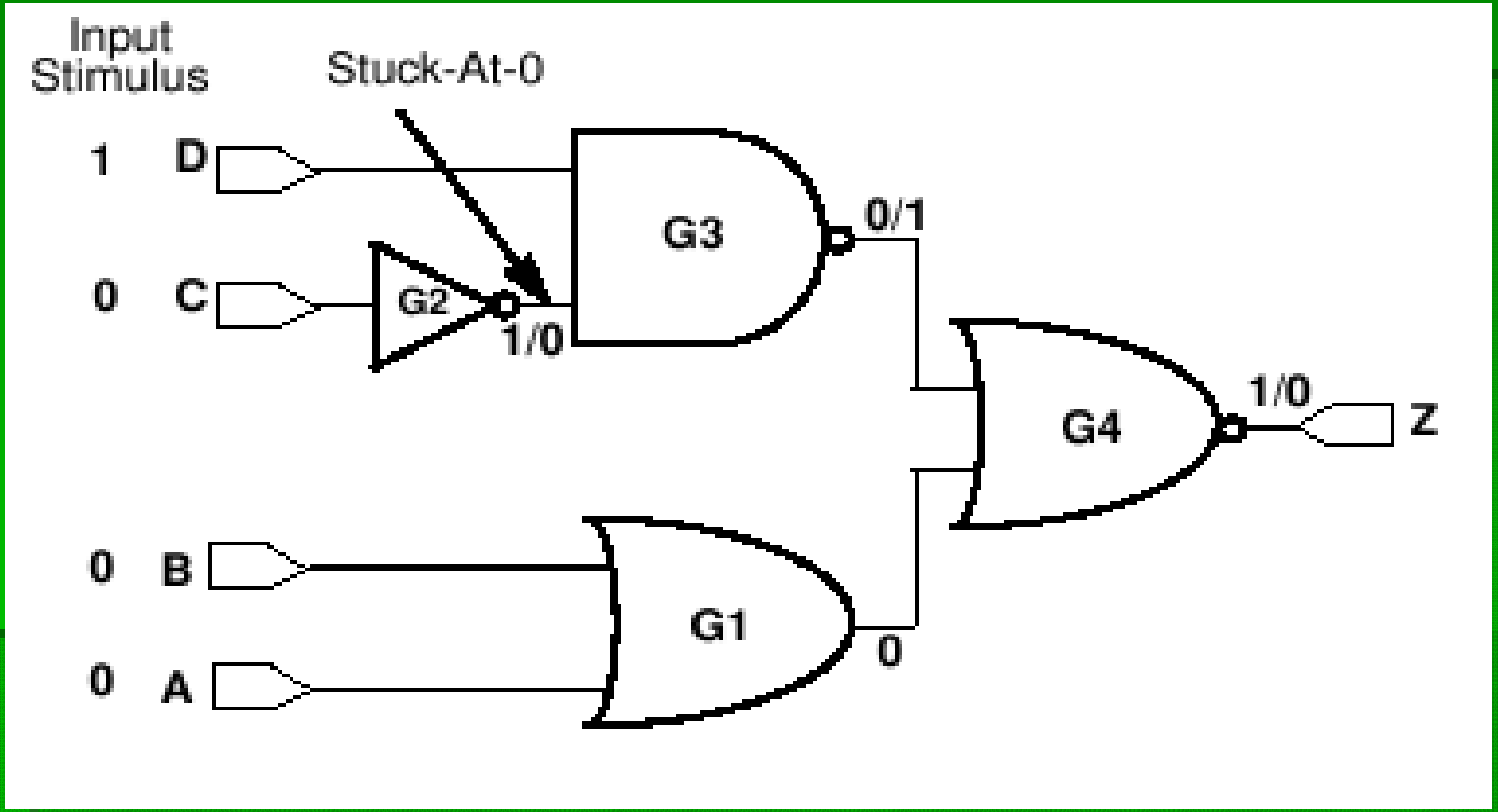
The stuck-at-0 model represents a signal that is permanently low regardless of the other signals that normally control the node. The stuck-at-1 model represents a signal that is permanently high regardless of the other signals that normally control the node.



# Detecting Stuck-At Faults

- The node of a stuck-at fault must be controllable and observable for the fault to be detected.
- To detect a stuck-at fault on a target node, you must do the following:
  - Control the target node to the opposite of the stuck-at value by applying data at the primary inputs.
  - Make the node's fault effect observable by controlling the value at all other nodes affecting the output response, so the targeted node is the active (controlling) node.

# Detecting Stuck-At Faults




*Simple Circuit With Detectable Stuck-at Fault*

# Fault Simulation

- Fault simulation detects a fault each time the output response of the faulty machine is a non-X value and is different from the output response of the good machine for a given vector.
- single stuck-at faults:
  - Stuck-at-1 on all pins of G1 (and ports A and B)
  - Stuck-at-1 on the input of G2 (and port C)
  - Stuck-at-0 on the inputs of G3 (and port D)
  - Stuck-at-1 on the output of G3
  - Stuck-at-1 on the inputs of G4
  - Stuck-at-0 on the output of G4 (and port Z)

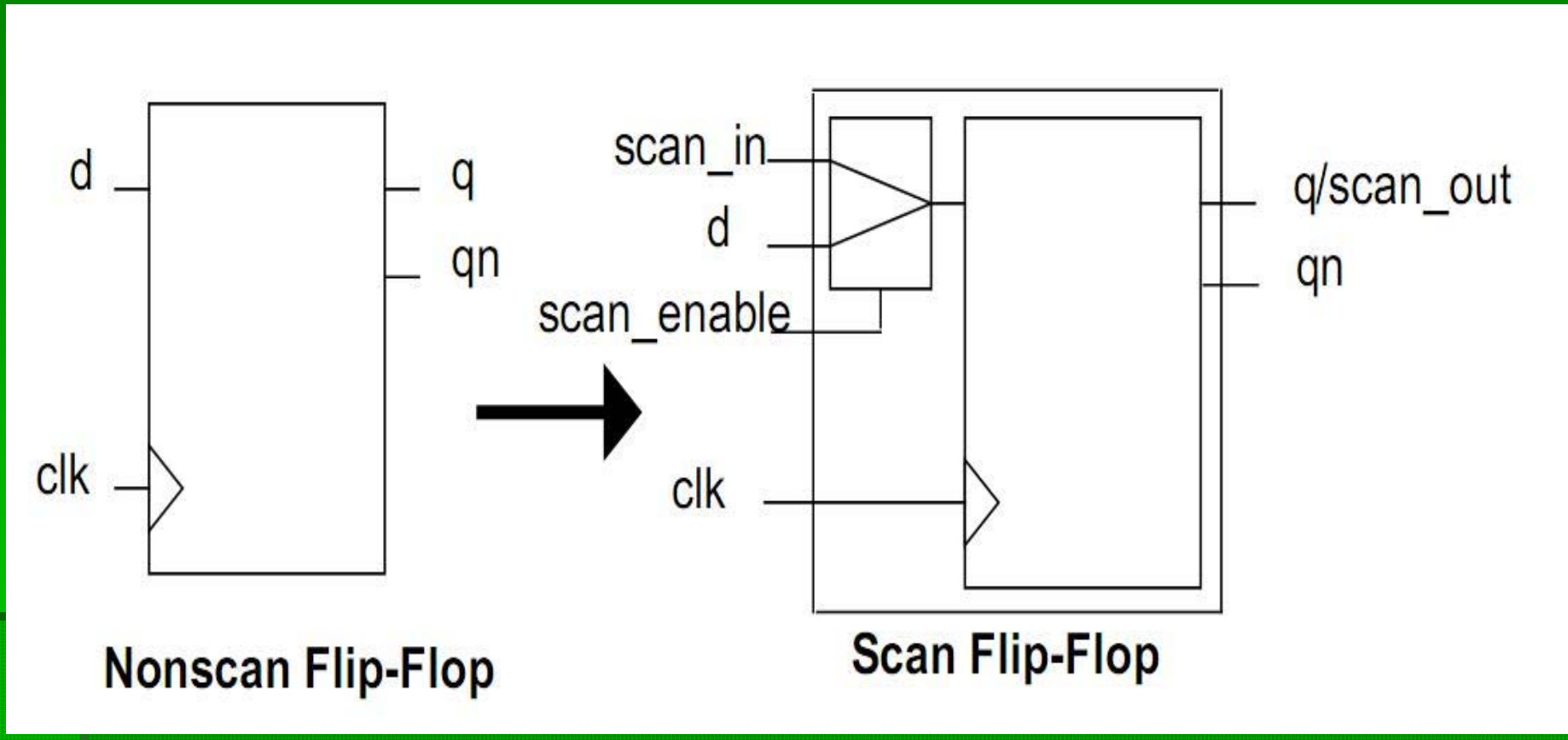
# Automatic Test Pattern Generation

- ATPG generates test patterns and provides test coverage statistics for the generated pattern set. For now, consider the term “test vector” to be the same as “test pattern.” ATPG for combinational circuits is well understood; it is usually possible to generate test vectors that provide high test coverage for combinational designs.
- After generating a vector, the tool fault-simulates the vector to determine the complete set of faults detected by the vector.

# Internal scan

- The principle of this technique is to modify the existing sequential elements in the design to support serial shift capability, in addition to their normal functions; and to connect these elements into serial chains to make, in effect, long shift registers.
- This technique simplifies the pattern generation problem by effectively dividing complex sequential designs into fully isolated combinational blocks (full-scan design) or semi-isolated combinational blocks (partial-scan design).

# Internal scan



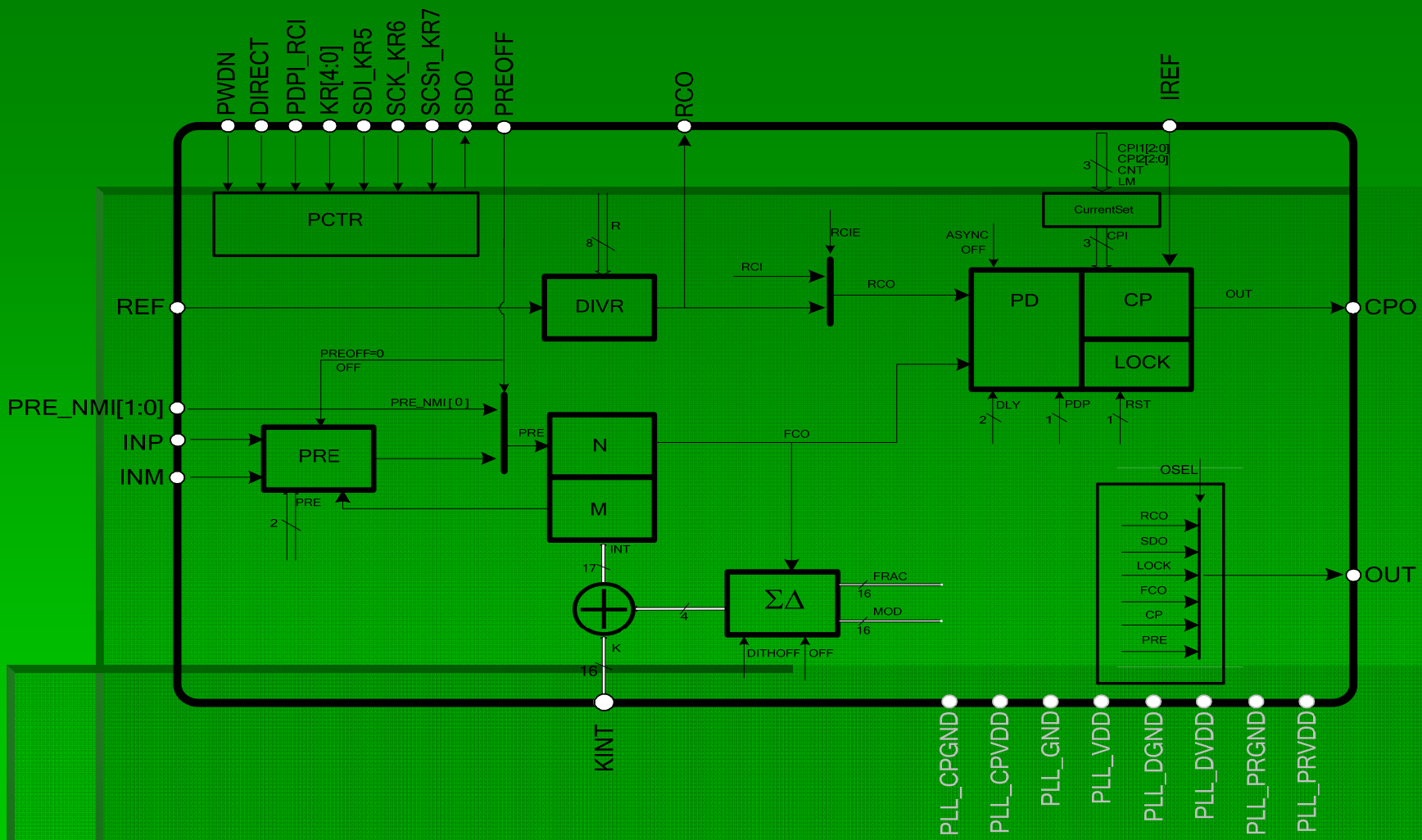

*D Flip-Flop With Scan Capability*

# Internal scan

- Adding scan circuitry to a design usually has the following effects:
- Design size and power increases slightly because scan cells are usually larger than the nonscan cells they replace, and the nets used for the scan signals occupy additional area.
- Design performance (speed) decreases marginally because of changes in the electrical characteristics of the scan cells that replace the nonscan cells.
- Global test signals that drive many sequential elements might require buffering to prevent electrical design rule violations.

# How to be, if technology ATPG for any reasons cannot be applied in the project???

So in the project of synthesizer PLL (Fig. 5 The functional diagramme of VLSI PLL) there are rigid frameworks on the occupied area the scheme on a crystal, and as on consumed energy. For this reason it became necessary working out of test scanned chains manually. Six various modes of testing, and as transition of all scheme in a test mode, by means of an operated code word in the interface used by the scheme have been provided. Thus, after transfer of all scheme in a test mode, it is necessary to choose which test mode it is necessary to start, that is to choose on what tested blocks to push generated by functional tests test-vector, how many steps to push a vector, and what scanned chains will be scan_out. Then the test vector on an exit is checked, being compared to result of the similar target channel in the functional test.




*The functional diagramme of VLSI PLL*

# Thank You!